



Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP#3	AZ DOUT ICH	Description	
0	0	RSVP	
0	1	Enter XOR Chain	
1	0	Normal Operation(default)	
1	1	Set PCIE port cofin bit1	

A16 swap override strap		
PCI_GNT#3	low = A16_swap_override_enable	
	high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

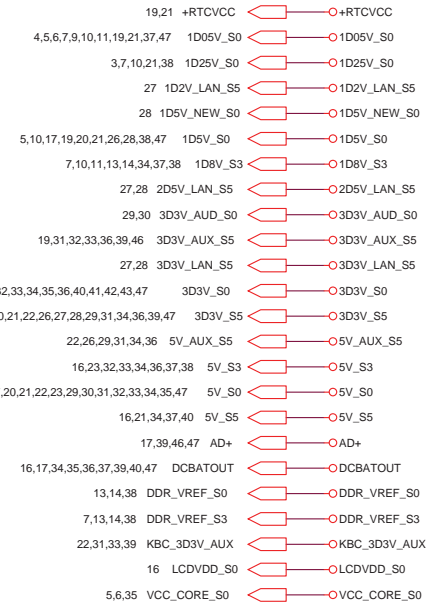
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

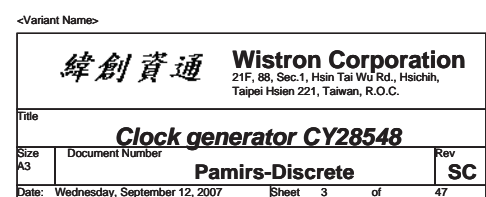
SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



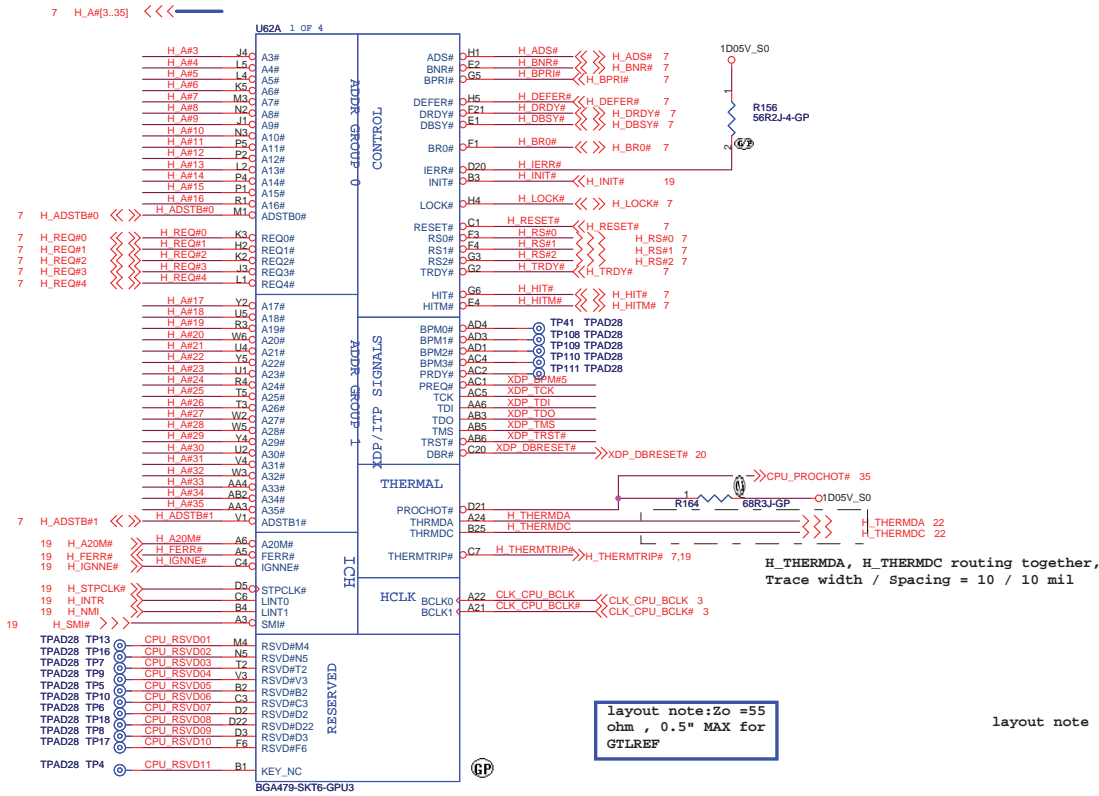
## INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes★ number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled★
CFG 19 DMI Lane Reserved	Normal Operation★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LH(0)	Reserved	
LH(1)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HL(11)	Normal Operation	

<Core Design>		
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Title		
Table of Content		
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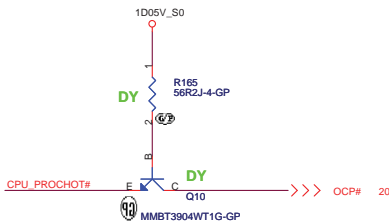
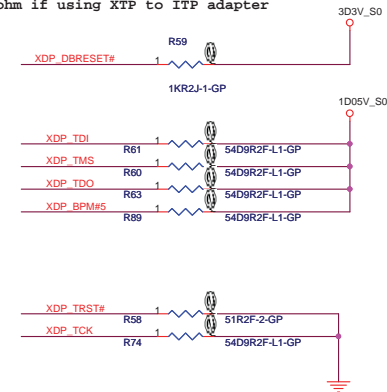


**WWW.AliSaler.Com**



original value:BGA479-SKT6-GPU1

layout note : Change R237 to 649 ohm if using XTP to ITP adapter



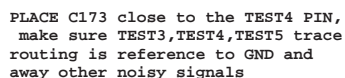
Title		Rev	
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Customer		Pamirs-Discrete	
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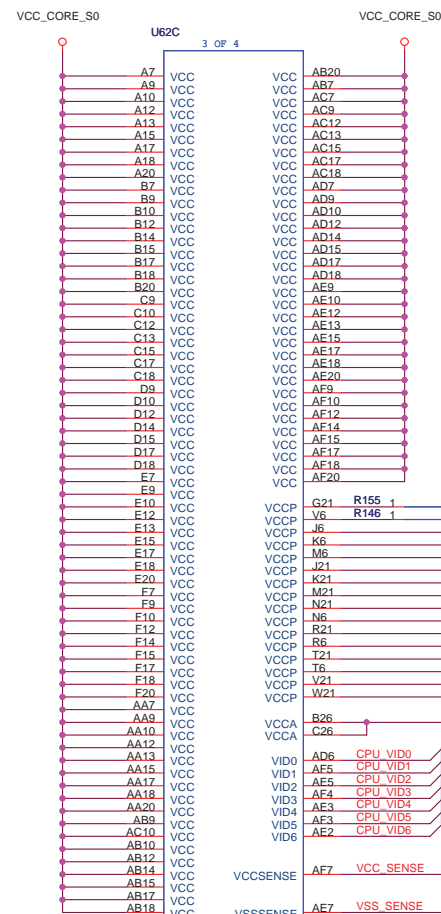
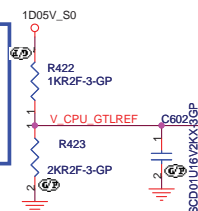
Merion(1/3)-AGTL+XDP

SC



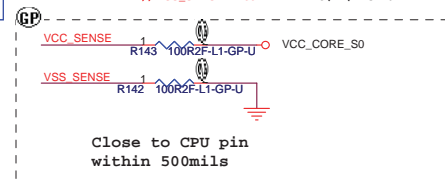
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Close to CPU  
pin AD26  
Z0=55 ohm  
with in  
500mils .



layout note:  
place C3 near  
PIN B26

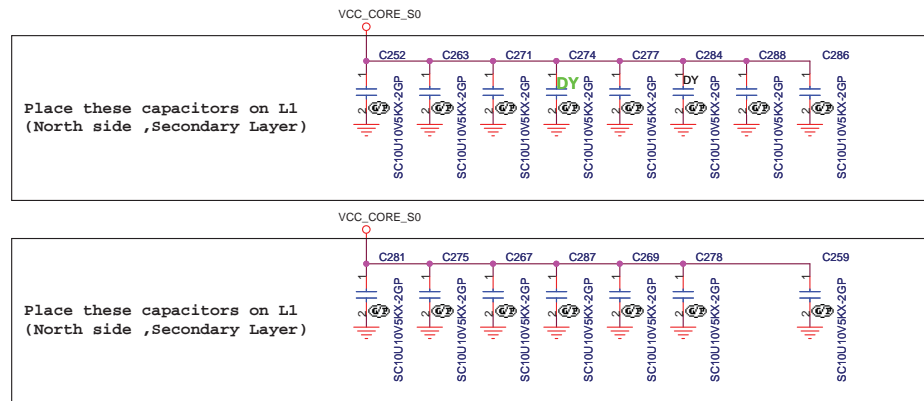
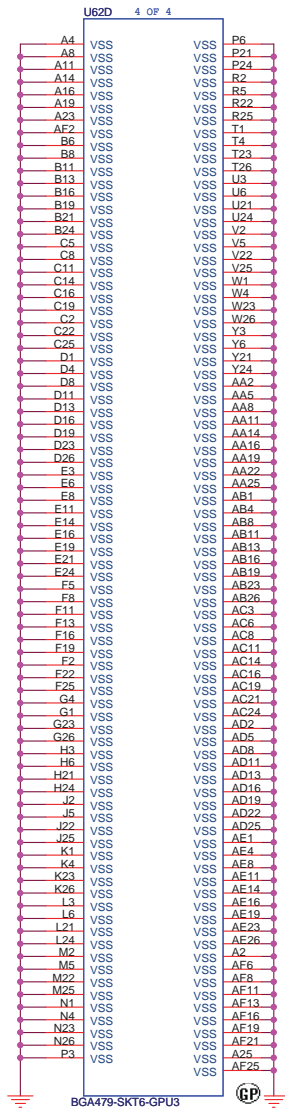
Length match within  
25 mils . The trace  
width/space/other is  
20/7/25 .



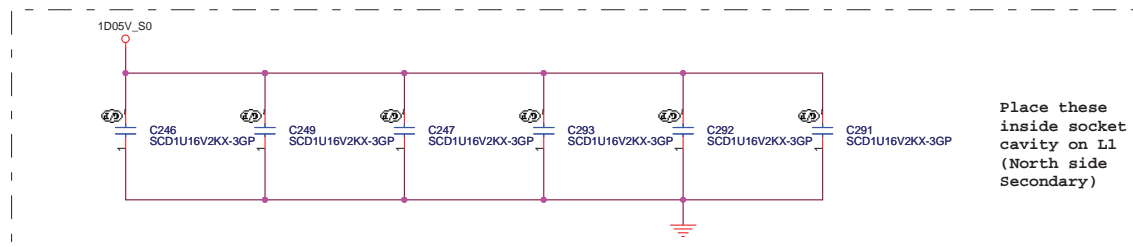
&lt;Core Design&gt;

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Title			
<b>Merou(2/3)-AGTL+PWR</b>			
Size	Document Number		Rev
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## Mid Frequend Decoupling



<Core Design>

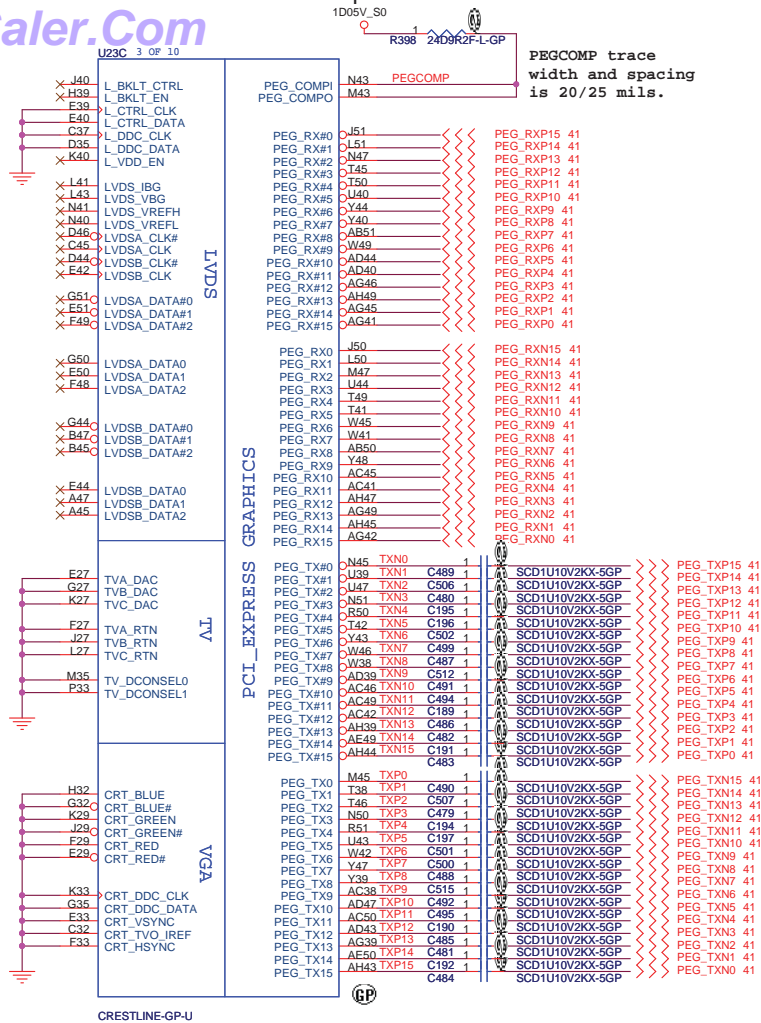
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Merion(3/3)-GND&amp;Bypass</b>	
Size A3	Document Number <b>Pamirs-Discrete</b>
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Rev <b>SC</b>	











CRESTLINE-GP-U

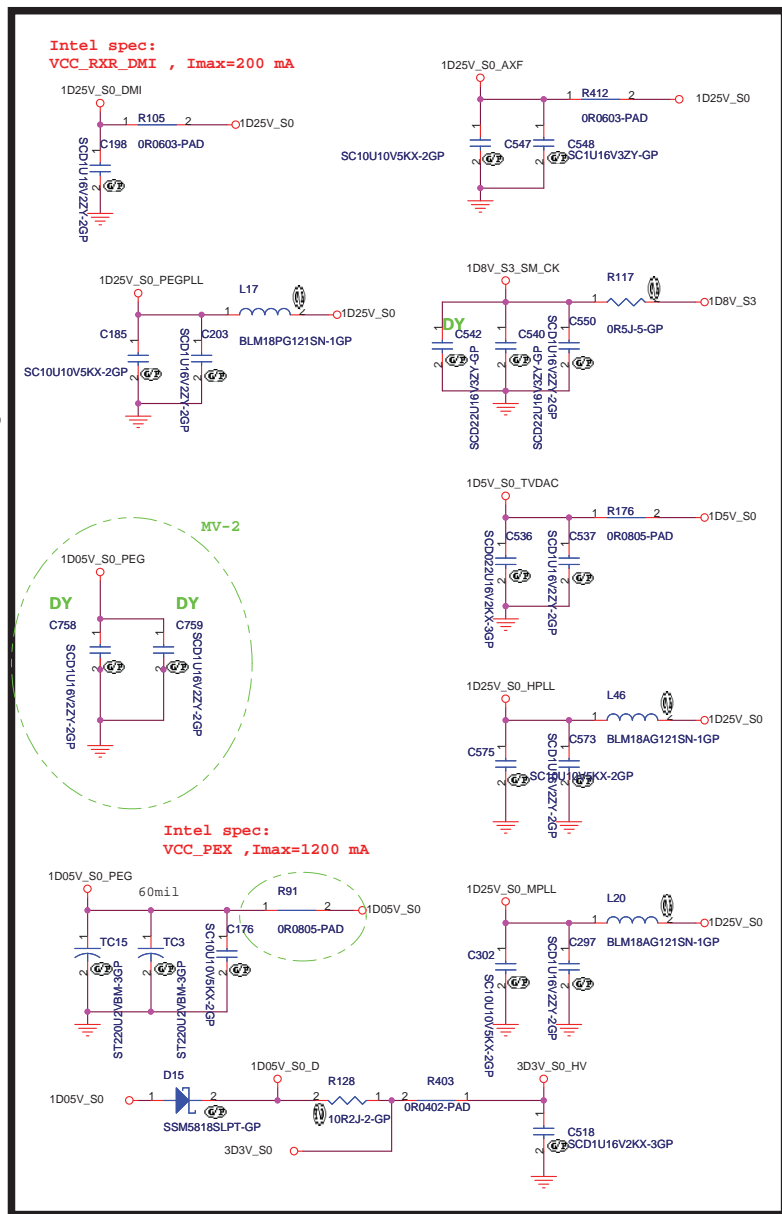
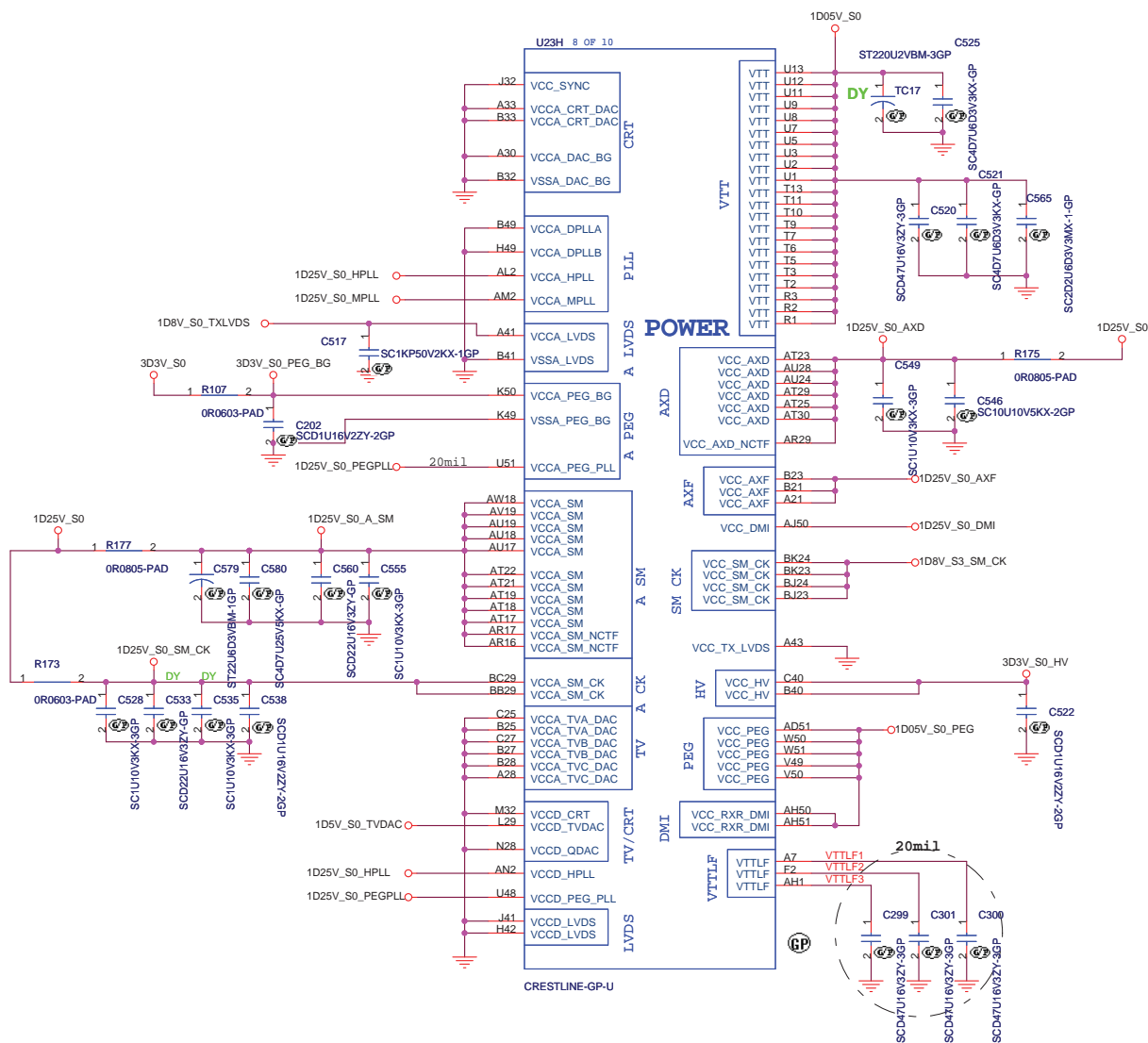
### Strap Pin Table

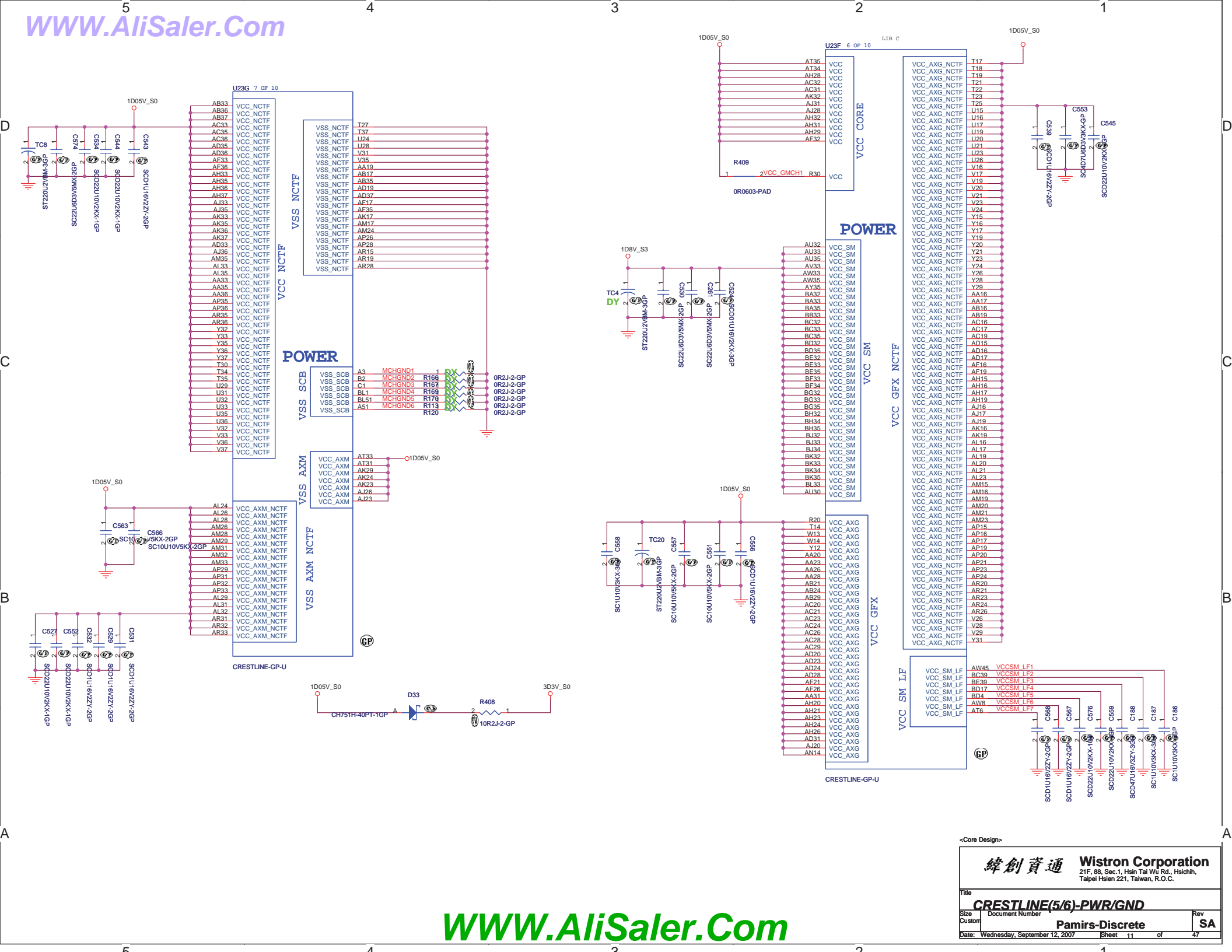
CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

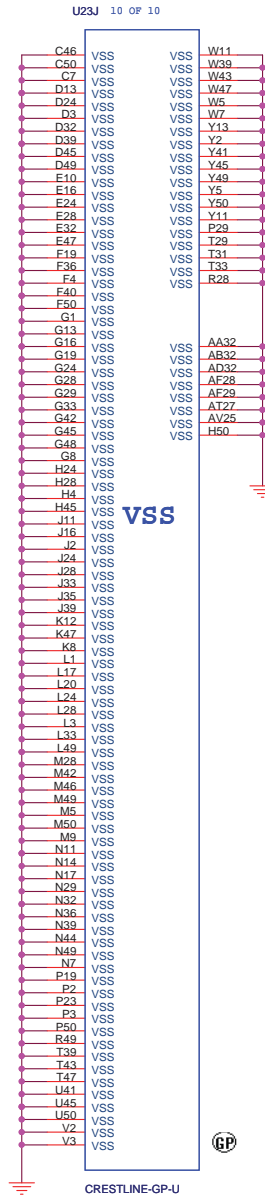
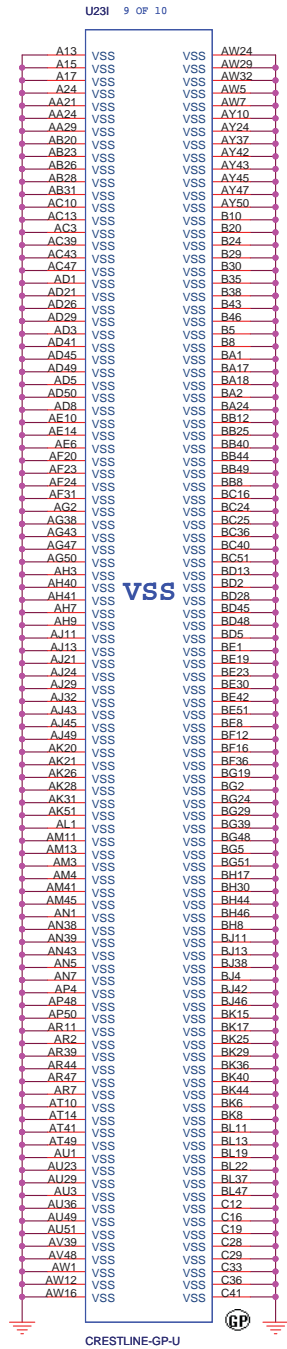
&lt;Core Design&gt;

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Title		
<b>CRESTLINE(3/6)-VGA/LVDS/TV</b>		
Size A3	Document Number	Rev
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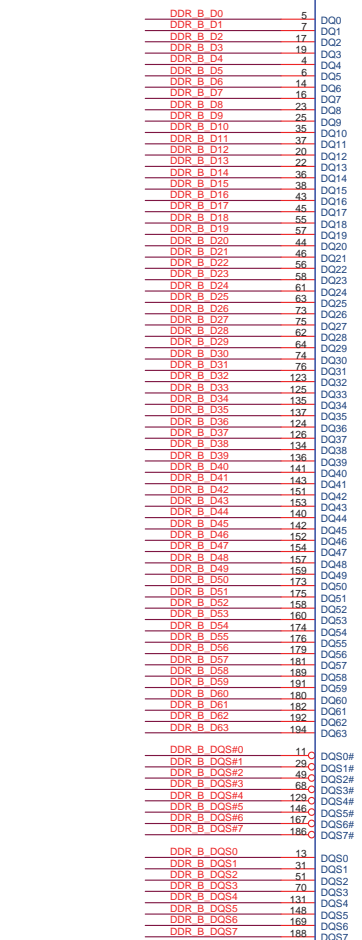
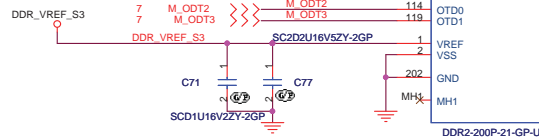
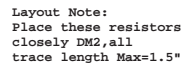
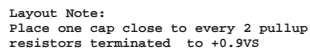
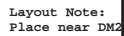


<Core Design>

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Title		
CRESTLINE(6/6)-PWR/GND		
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Layout Note:  
Place these resistors  
closely DM1,all  
trace length Max=1.5"





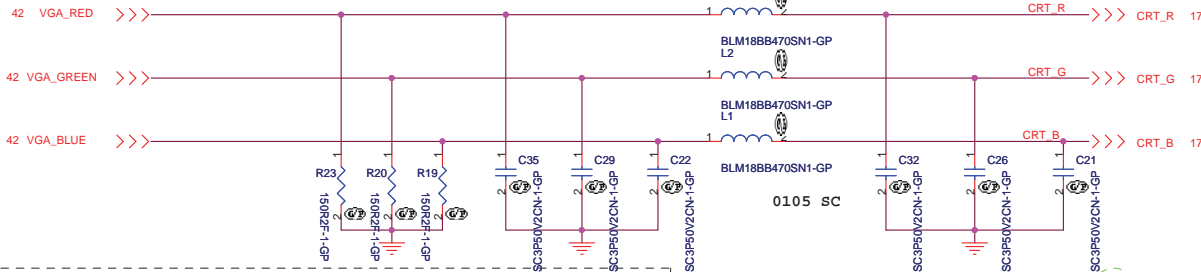
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>DDRII-SODIMM SLOT2</b>			
Size	Document Number		Rev
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# CRT I/F & CONNECTOR

Layout Note:  
Place these resistors  
close to the CRT-out  
connector



**Layout Note:**  
\* Must be a ground return path between this ground and the ground on the VGA connector.  
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

CRT LEAKAGE 0914

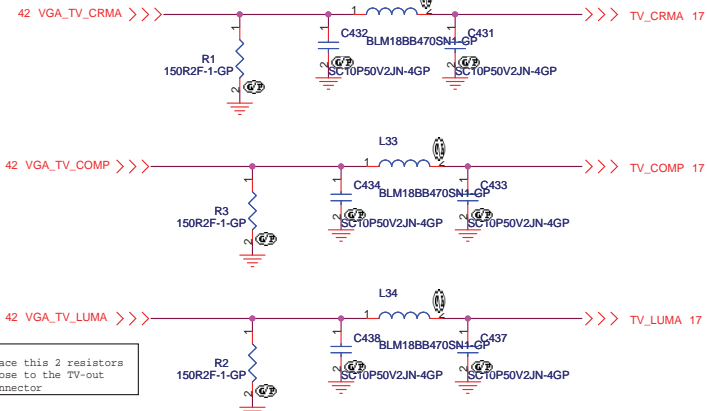
0R24-2-GP  
R665

17,42 GMCH\_HSYNC >>>

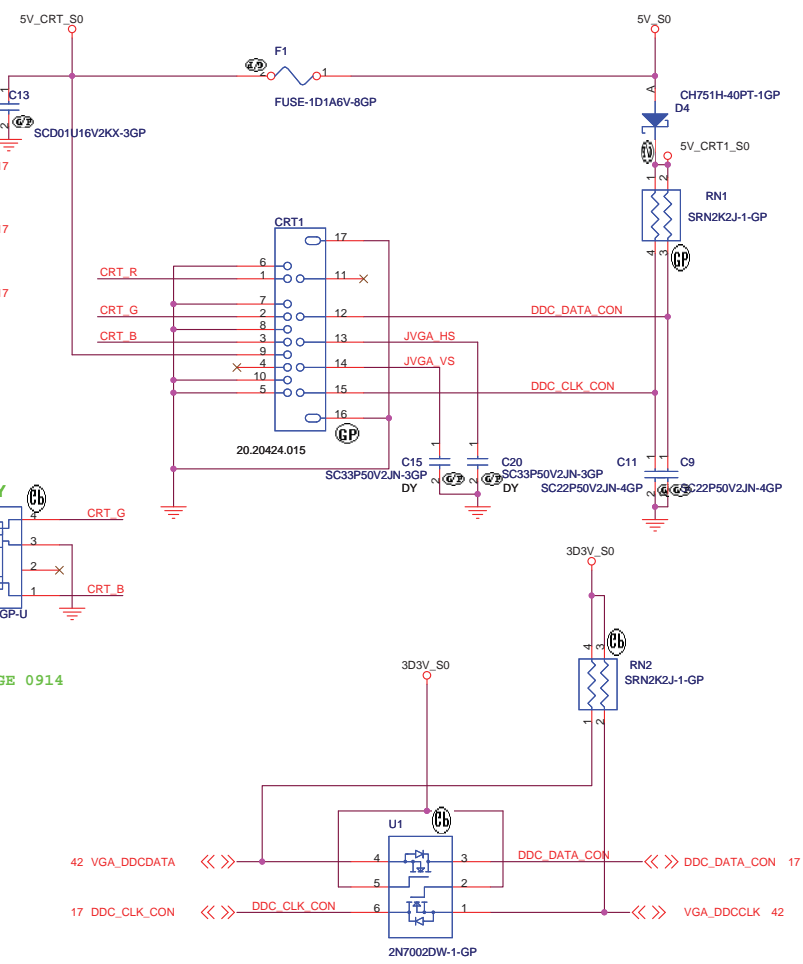
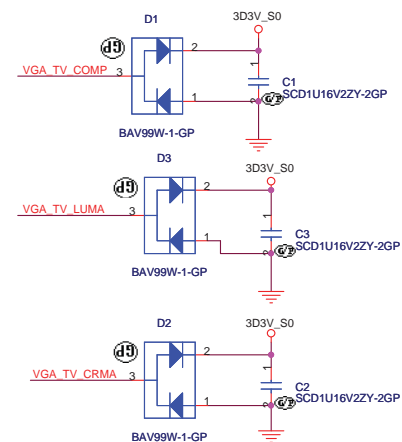
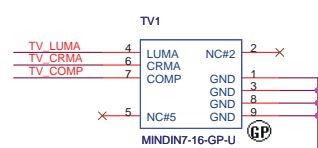
17,42 GMCH\_VSYNC >>>

## TV OUT CONN

connector



Place this 2 resistors  
close to the TV-out  
connector



5V @ ext. CRT side

<Core Design>

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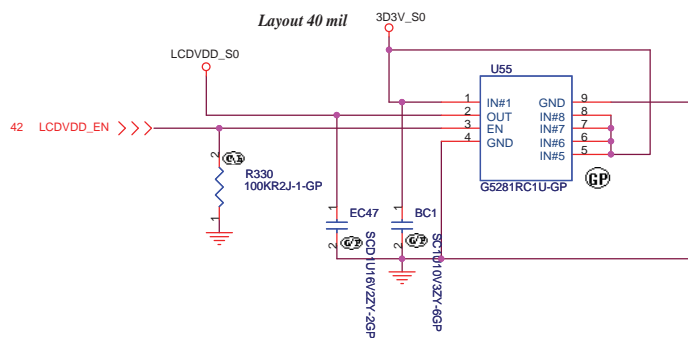
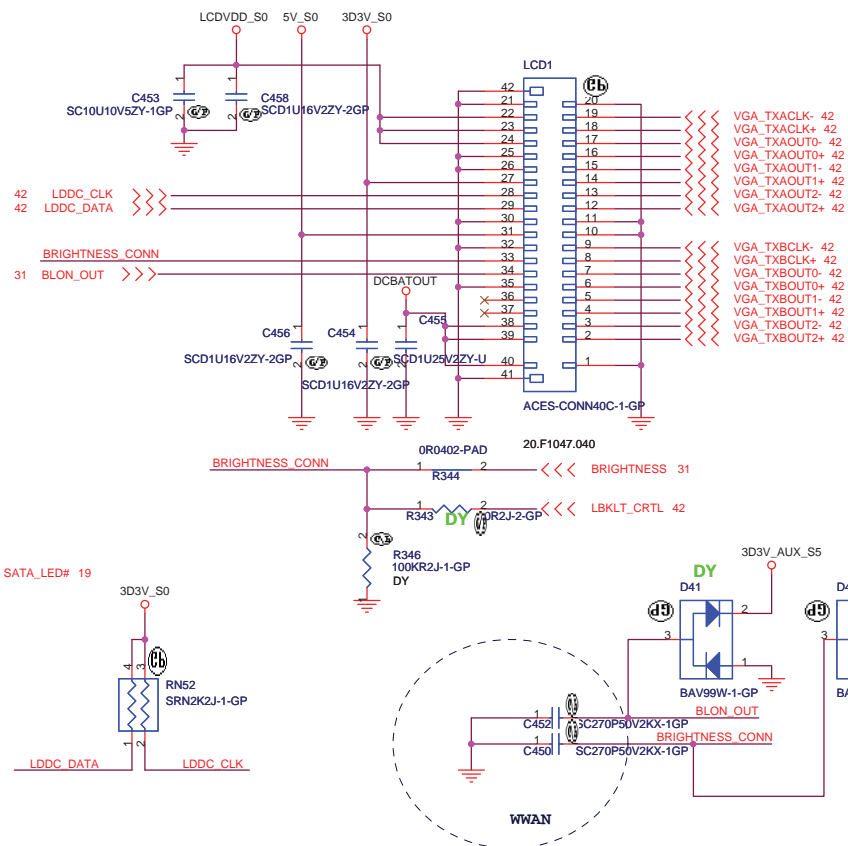
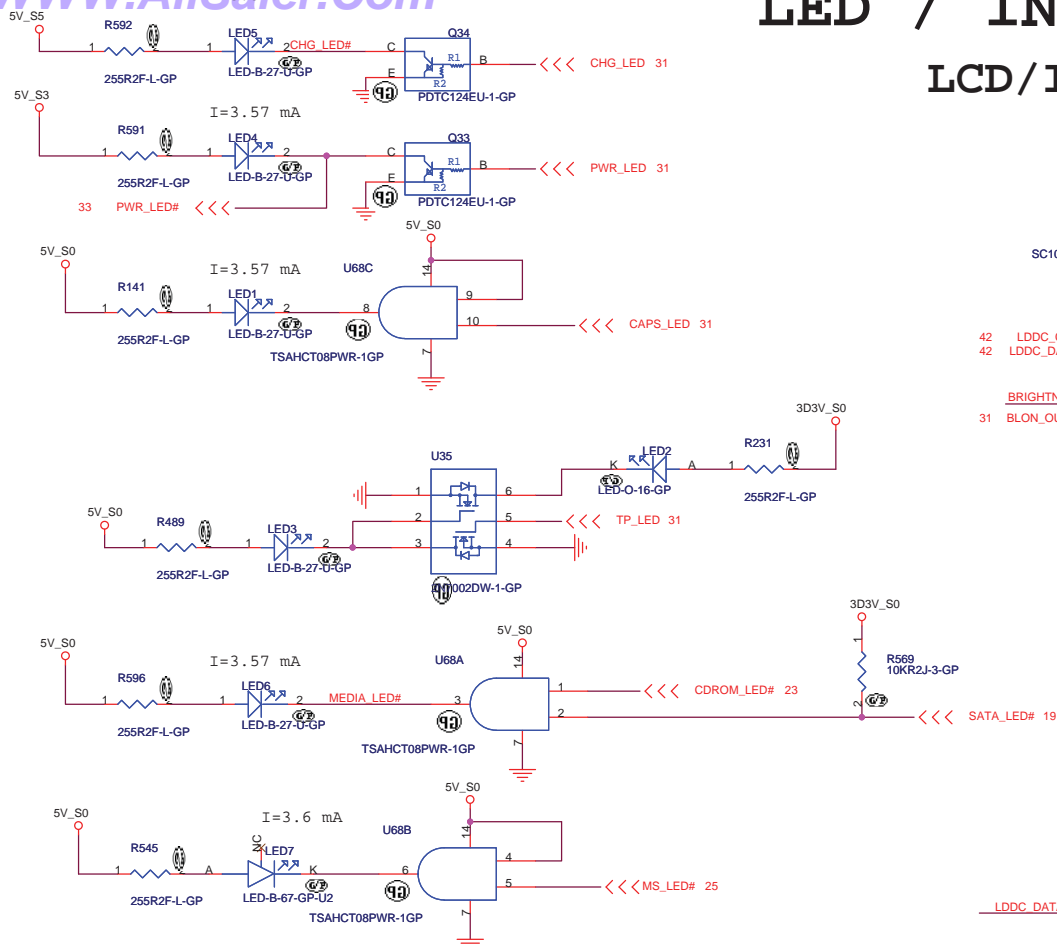
Title: **CRT/TV Connector**

Size A3 Document Number: **Pamirs-Discrete** Rev: **SA**

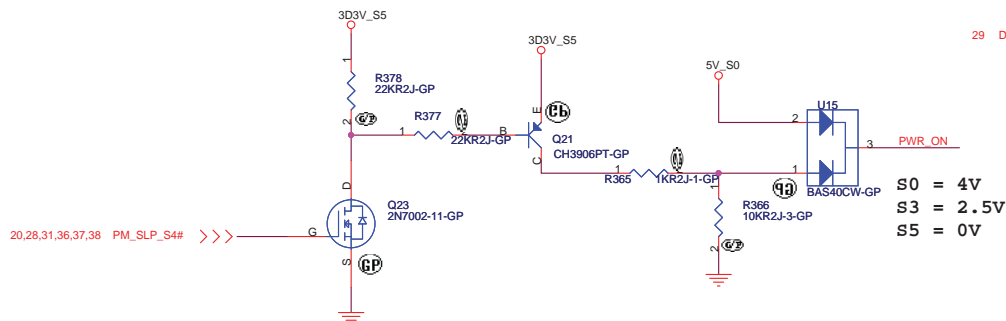
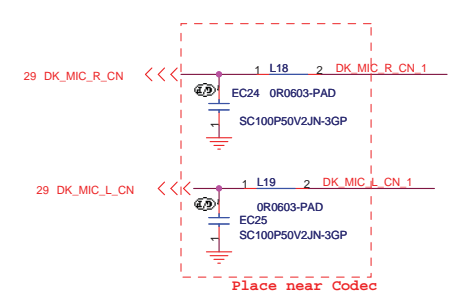
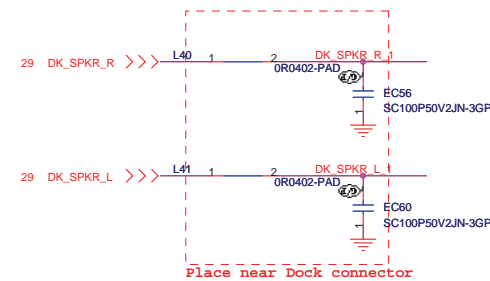
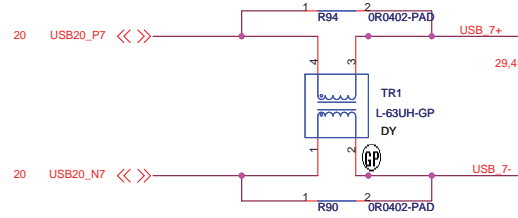
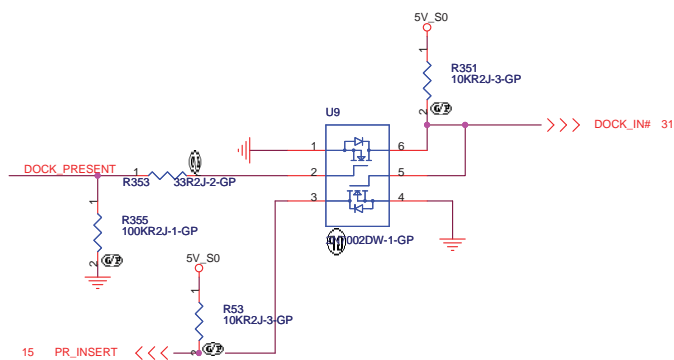
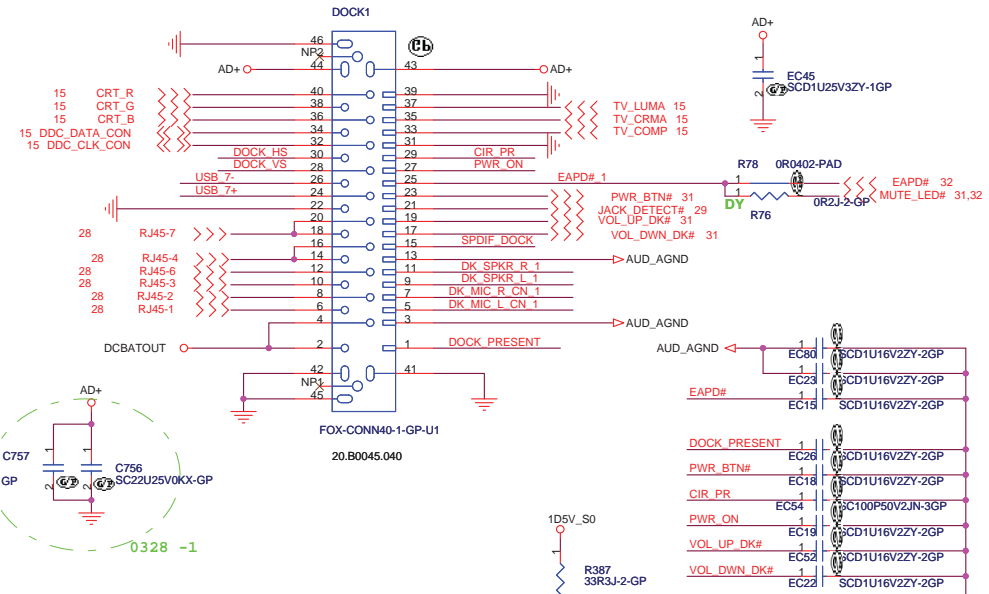
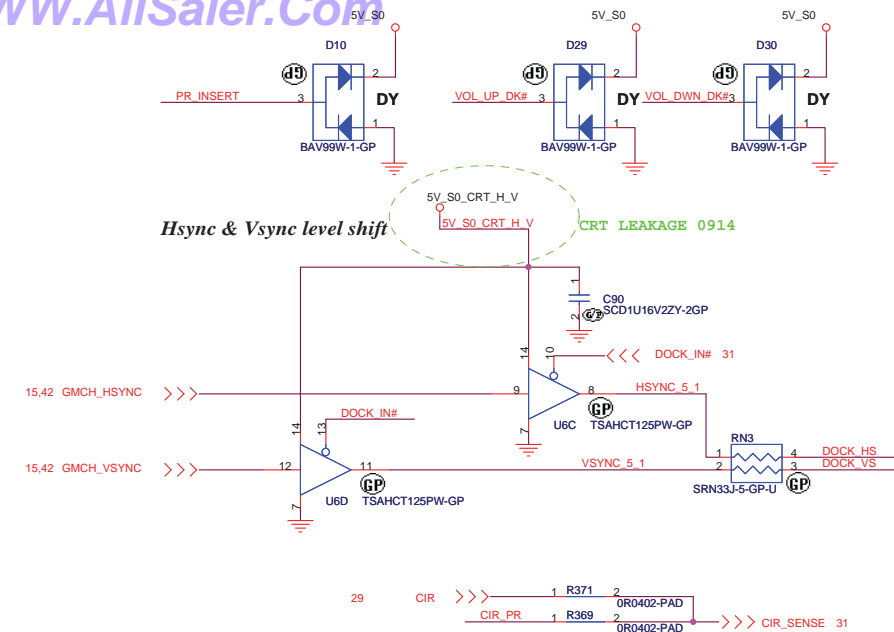
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# LED / INVERTER INTERFACE

## LCD/INV CONN



<div style="display: flex; justify-content: space-between; align-items: center;"> <span>&lt;Core Design&gt;</span> <div style="text-align: center;">  <p><b>緯創資通</b></p> <p><b>Wistron Corporation</b></p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p> </div> </div>				
Title				
<b>LCD/Inverter Connector</b>				
Size Custom	Document Number	<b>Pamirs-Discrete</b>		Rev <b>SA</b>
Date:	Wednesday, September 12, 2007	Sheet	16 of	47

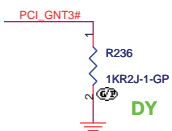
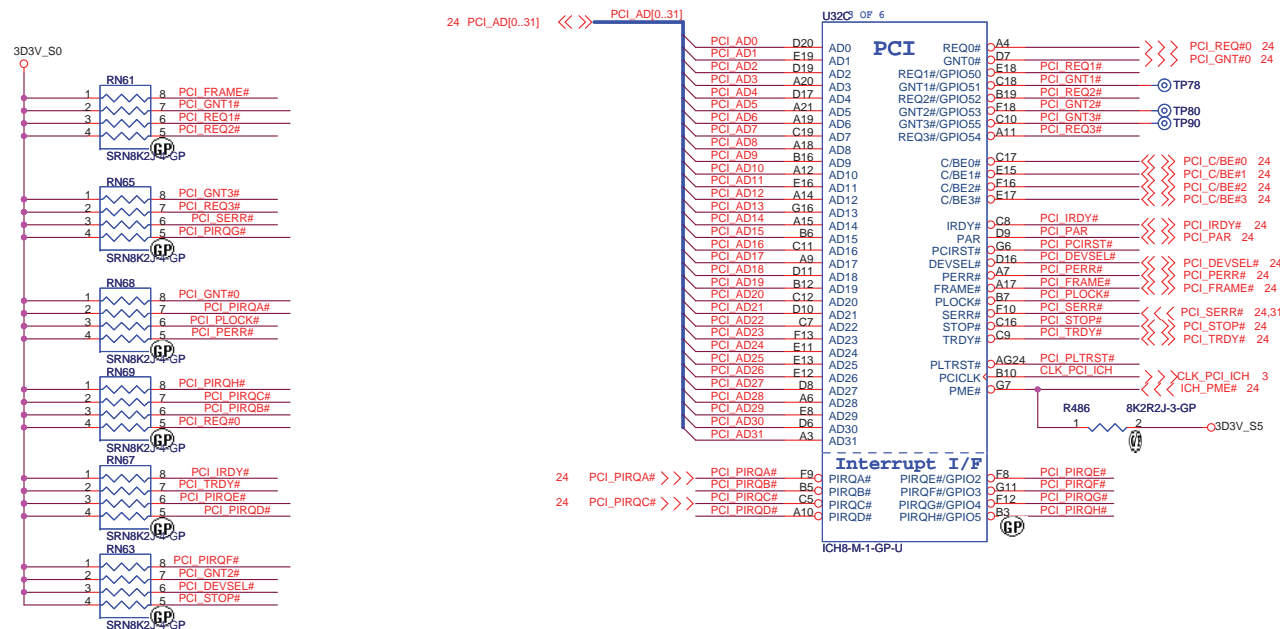


S0 = 4V  
S3 = 2.5V  
S5 = 0V

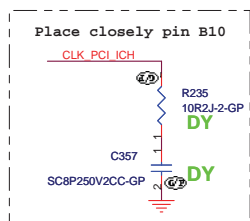
&lt;Core Design&gt;

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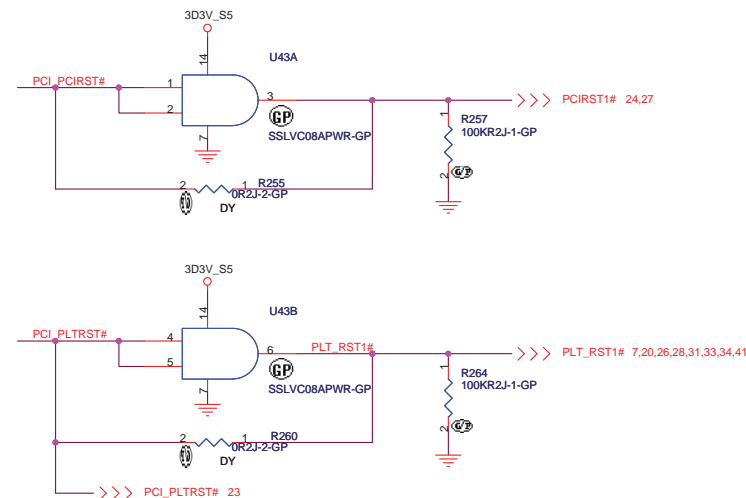
Title			
<b>Board to board conn/ Docking</b>			
Size A3	Document Number		Rev
	<b>Pamirs-Discrete</b>		<b>SA</b>
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A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



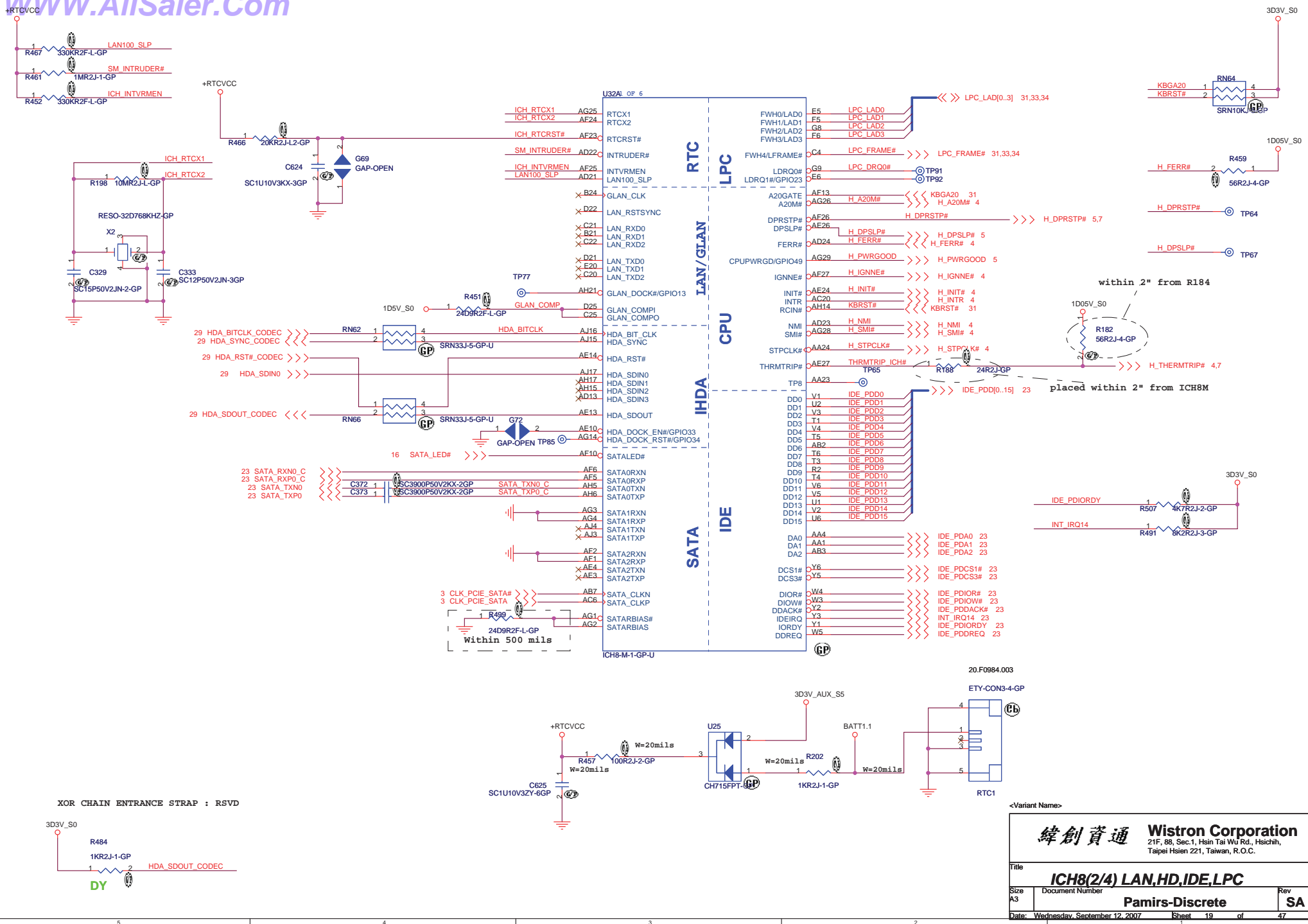
<Variant Name>

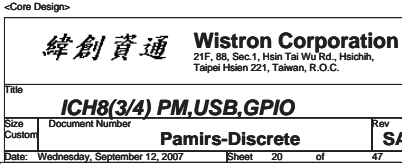
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Title: **ICH8(1/4)-PCI/INT**

Size A3 Document Number: **Pamirs-Discrete** Rev: **SA**

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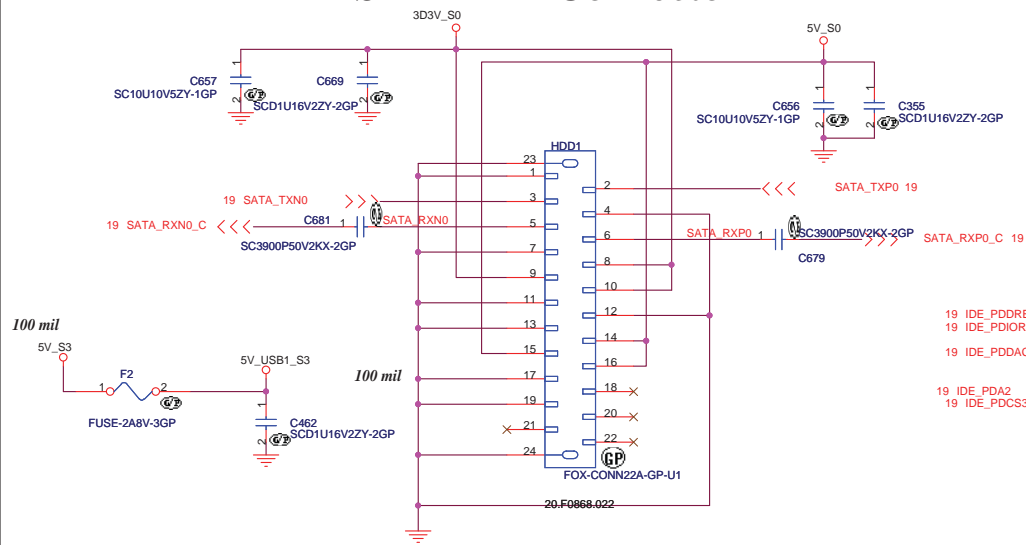




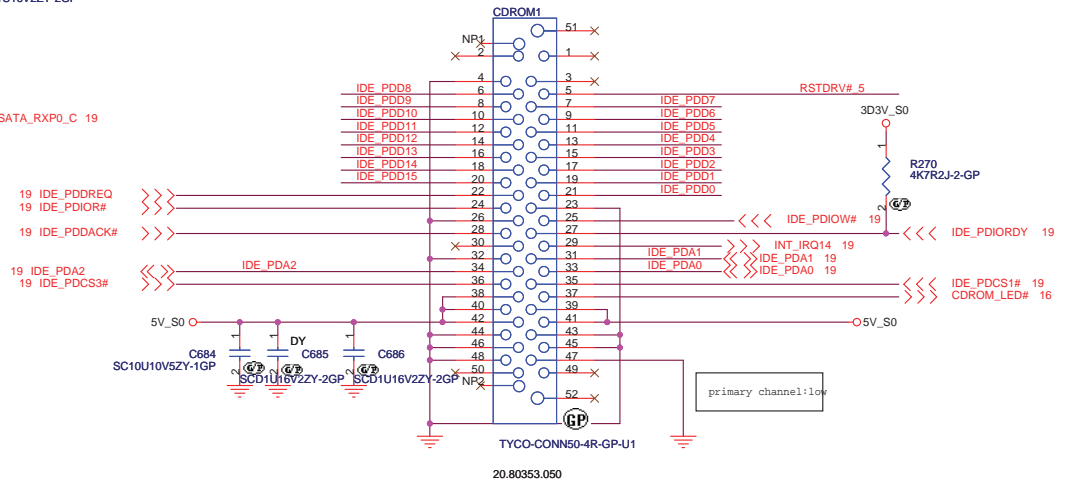




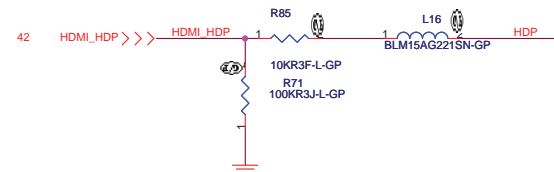
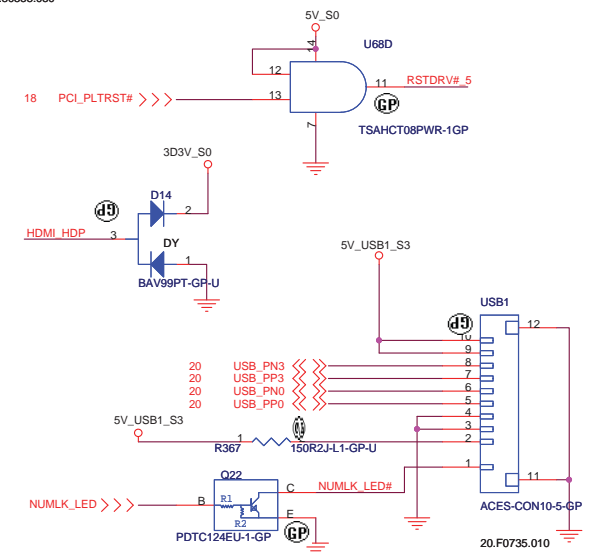
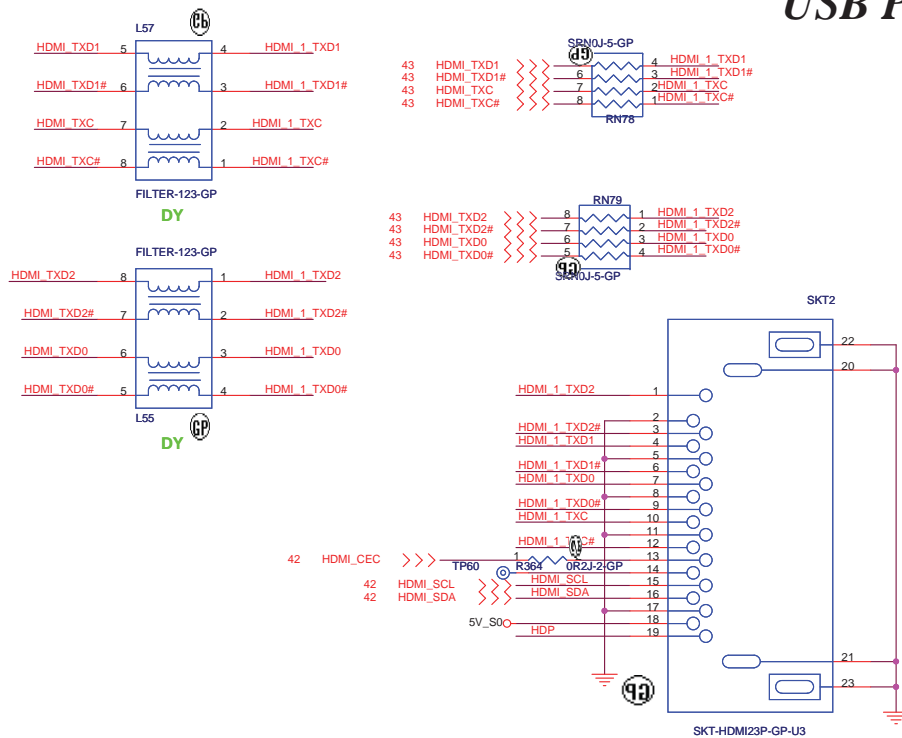
## SATA HD Connector




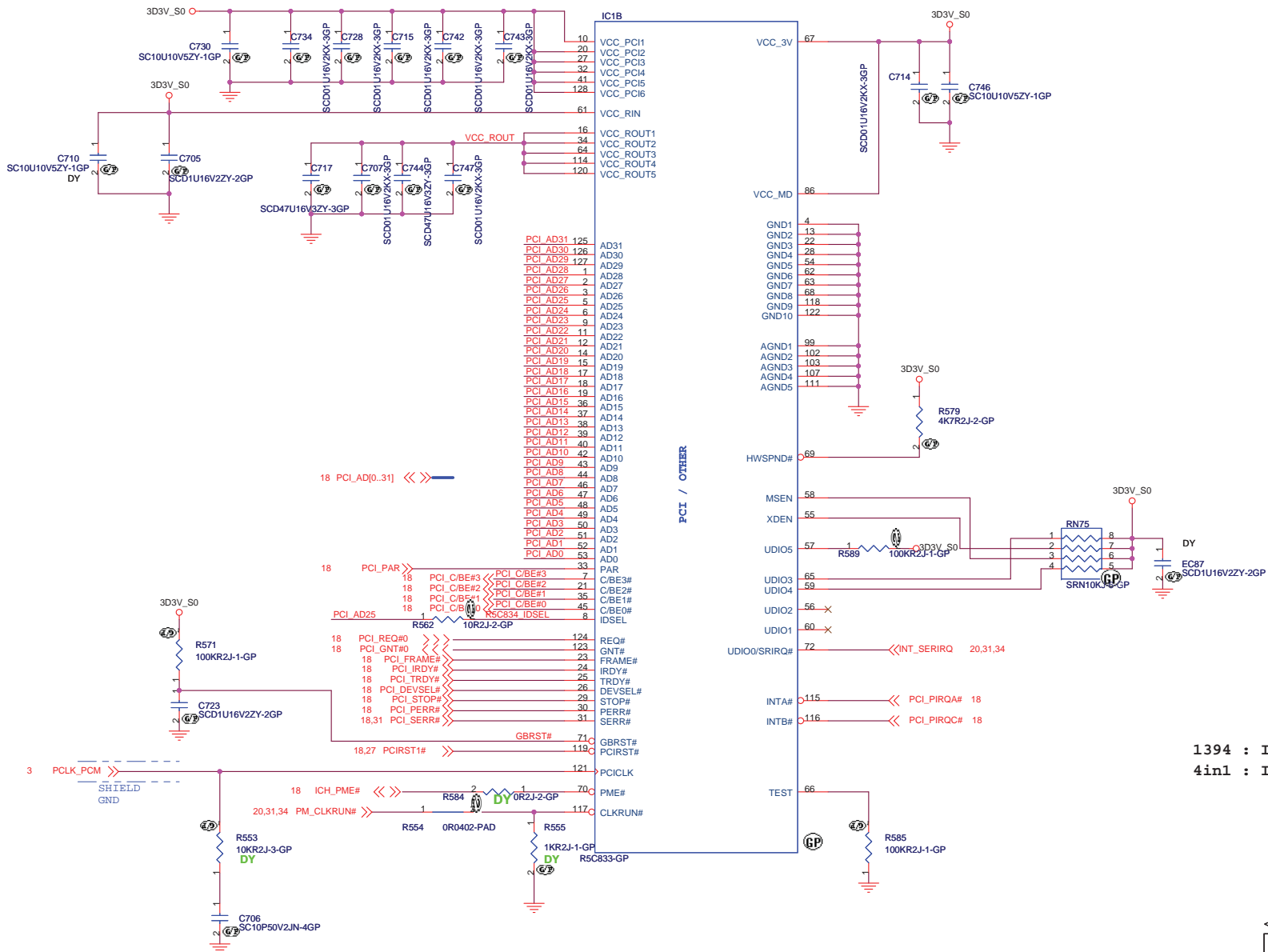
## CD-ROM CONNECTOR



## USB PORT

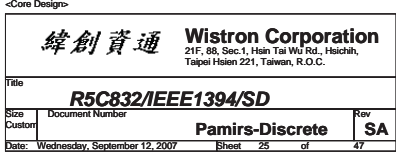


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Title			
<div> <b>HD/CDROM/USB</b> </div>			
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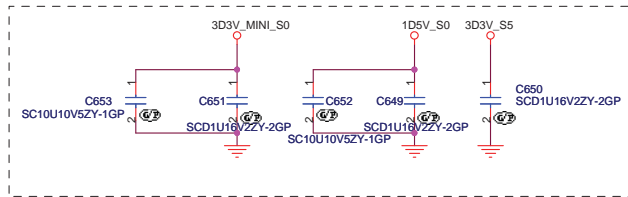
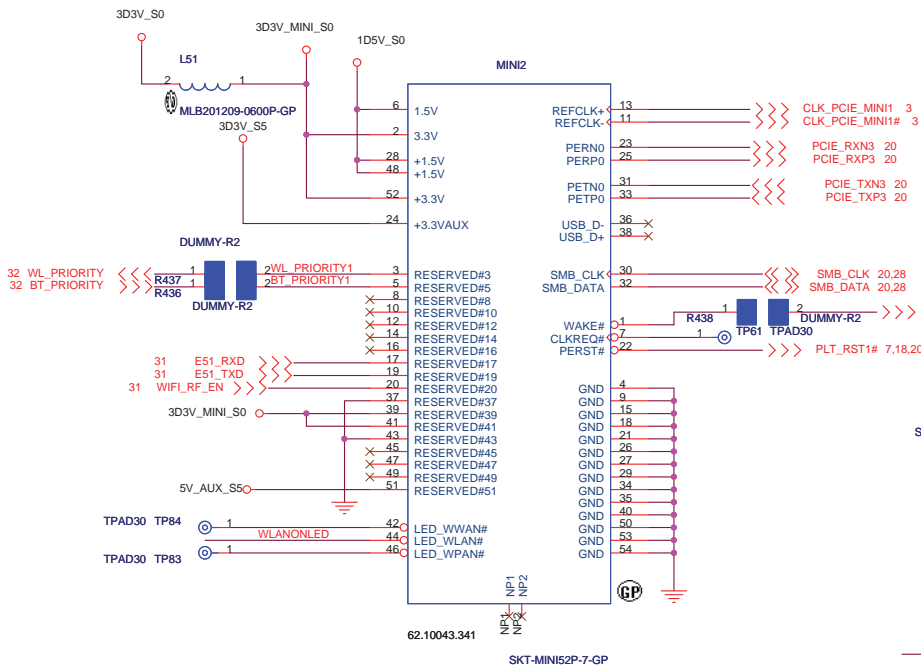
<Core Design>

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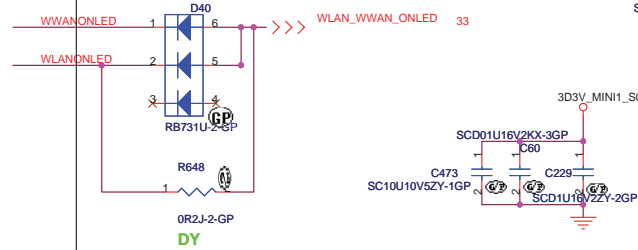
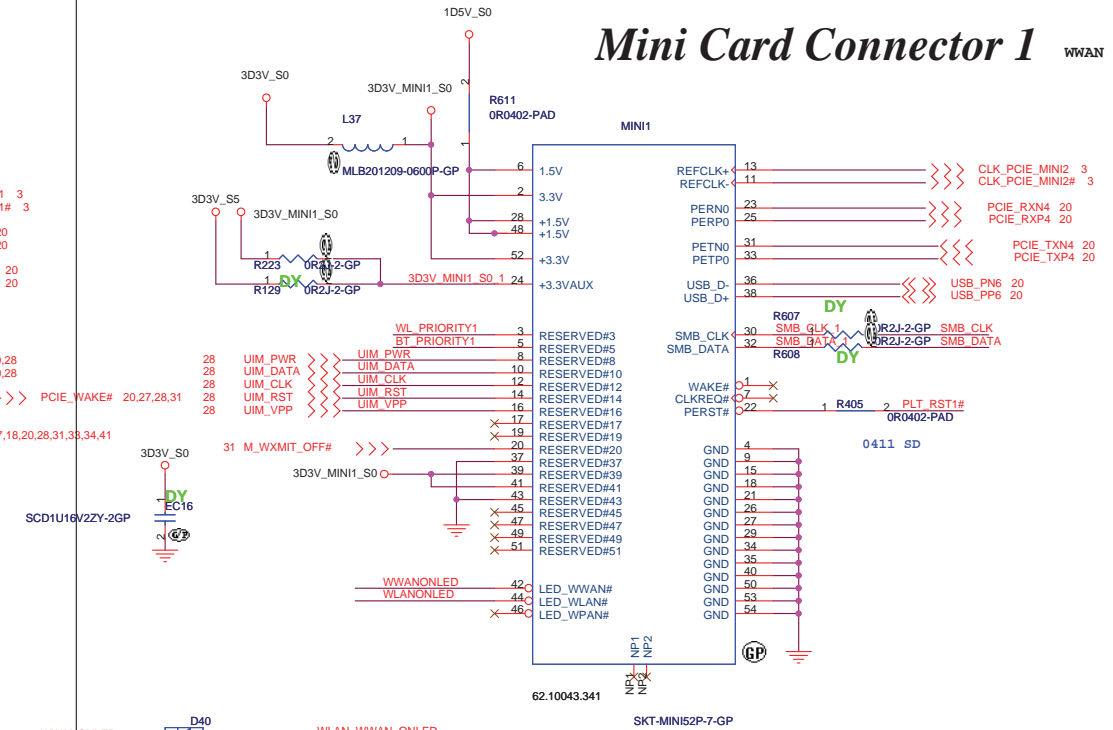
# Mini Card Connector 2

Wireless card



# Mini Card Connector 1

WWAN

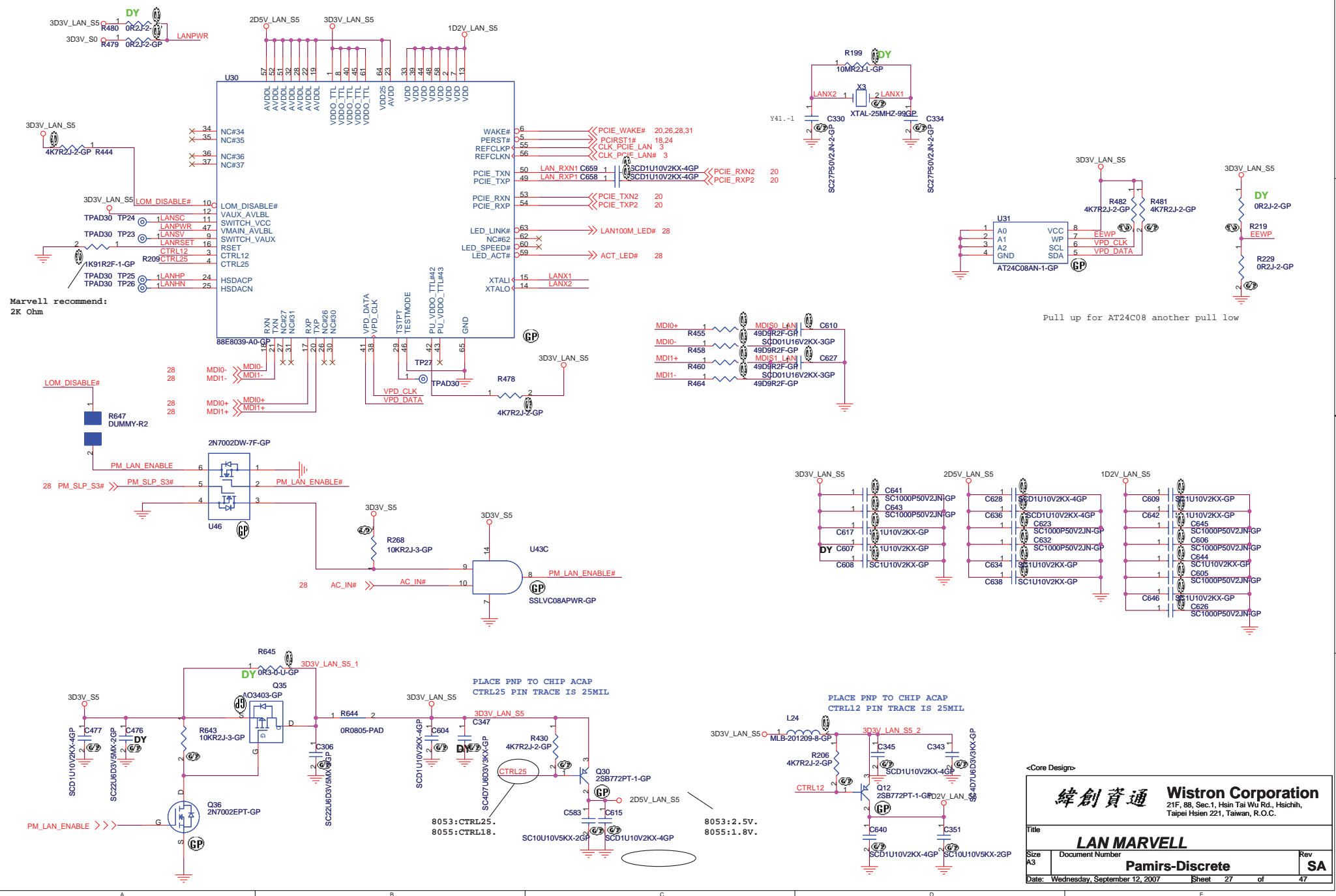


<Core Design>

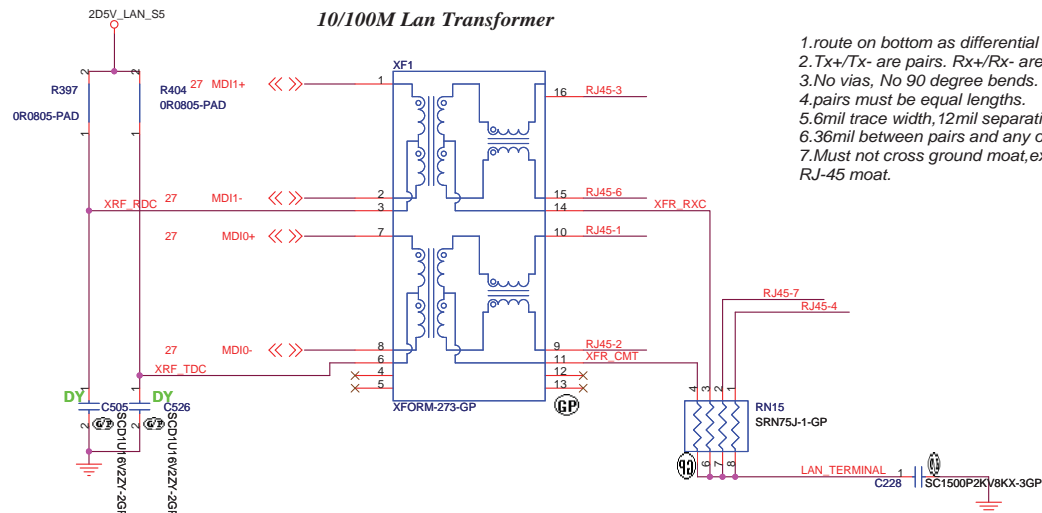
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Title	MINI CARD CONN.		
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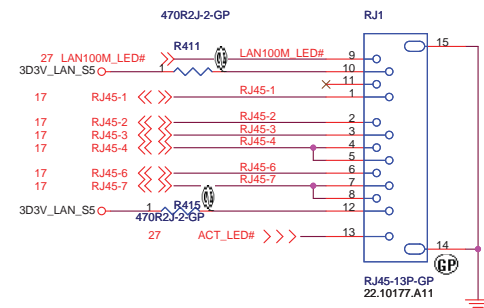


### 10/100M Lan Transformer



- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

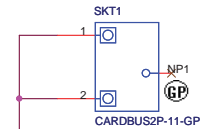
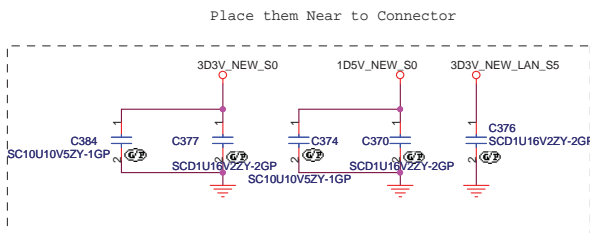
PIN09 : GREEN  
PIN11 : ORANGE  
PIN13 : YELLOW



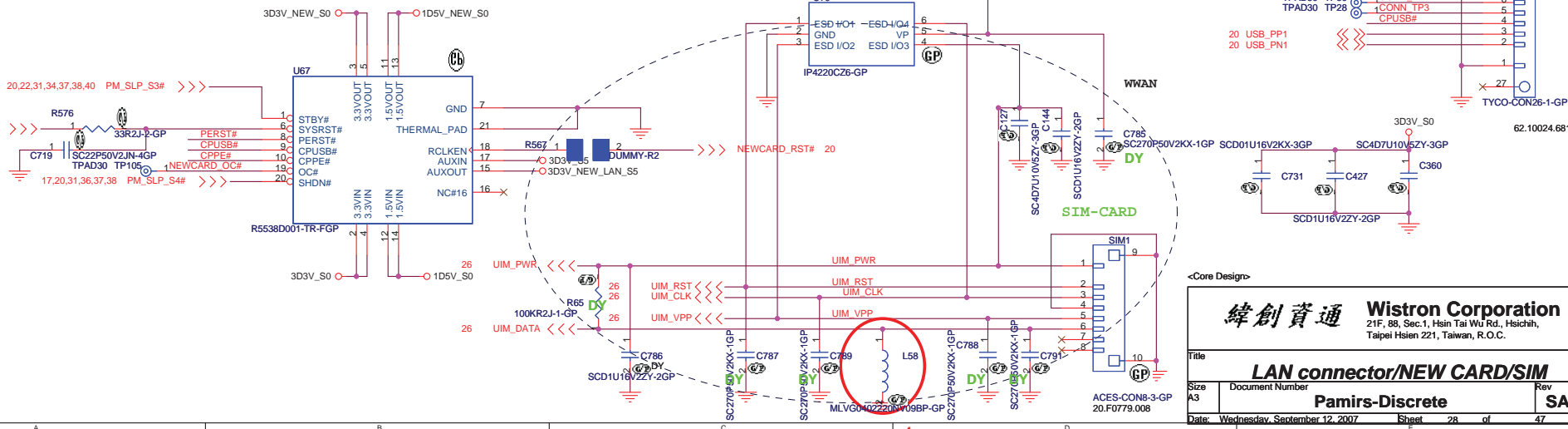
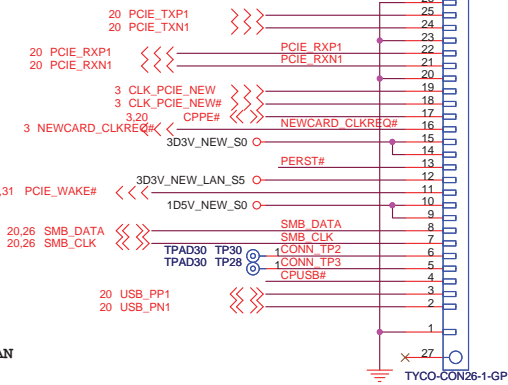
Green : Link up  
Blinking : TX/RX activity

### NEWCARD Connector

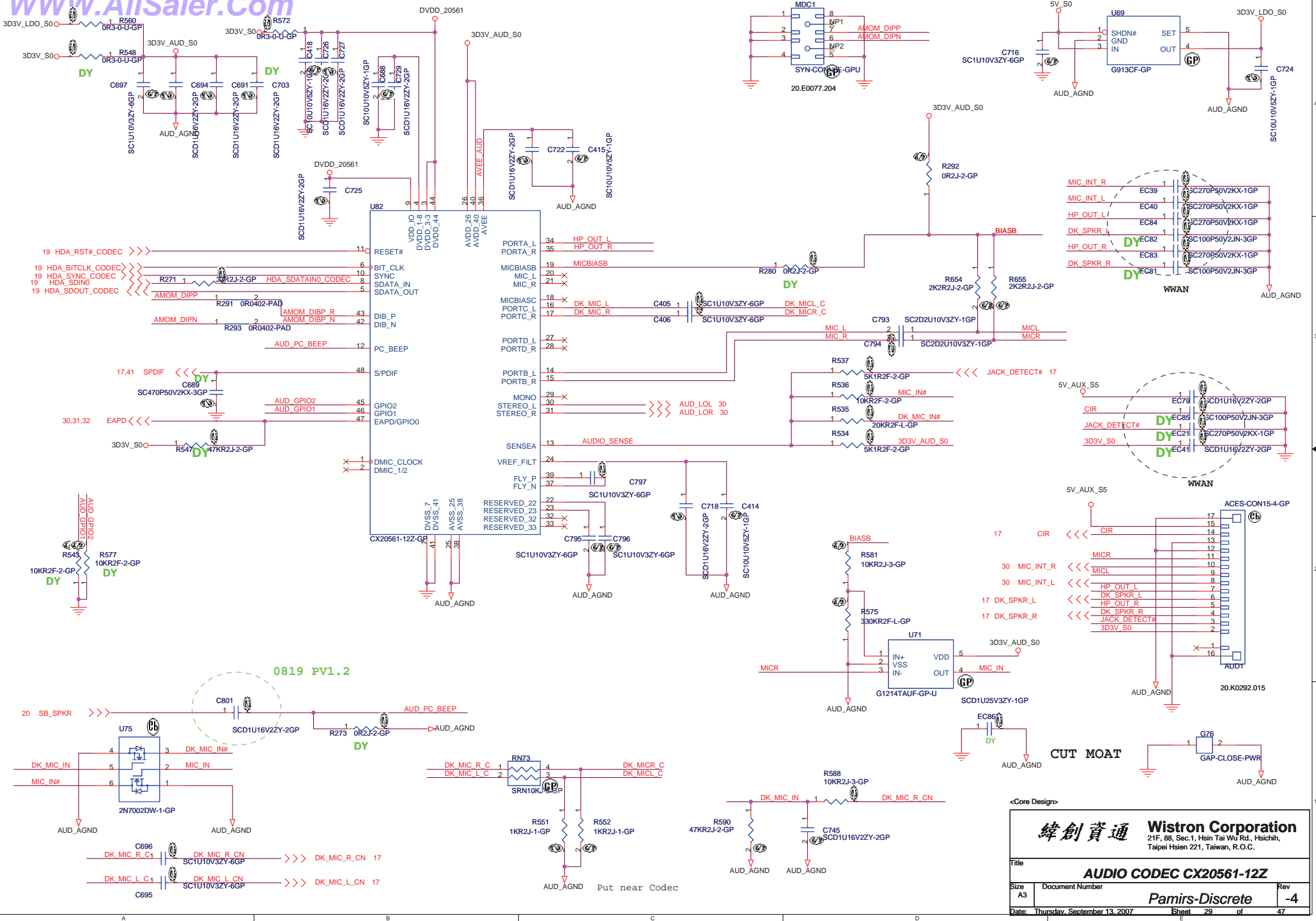
Place them Near to Chip

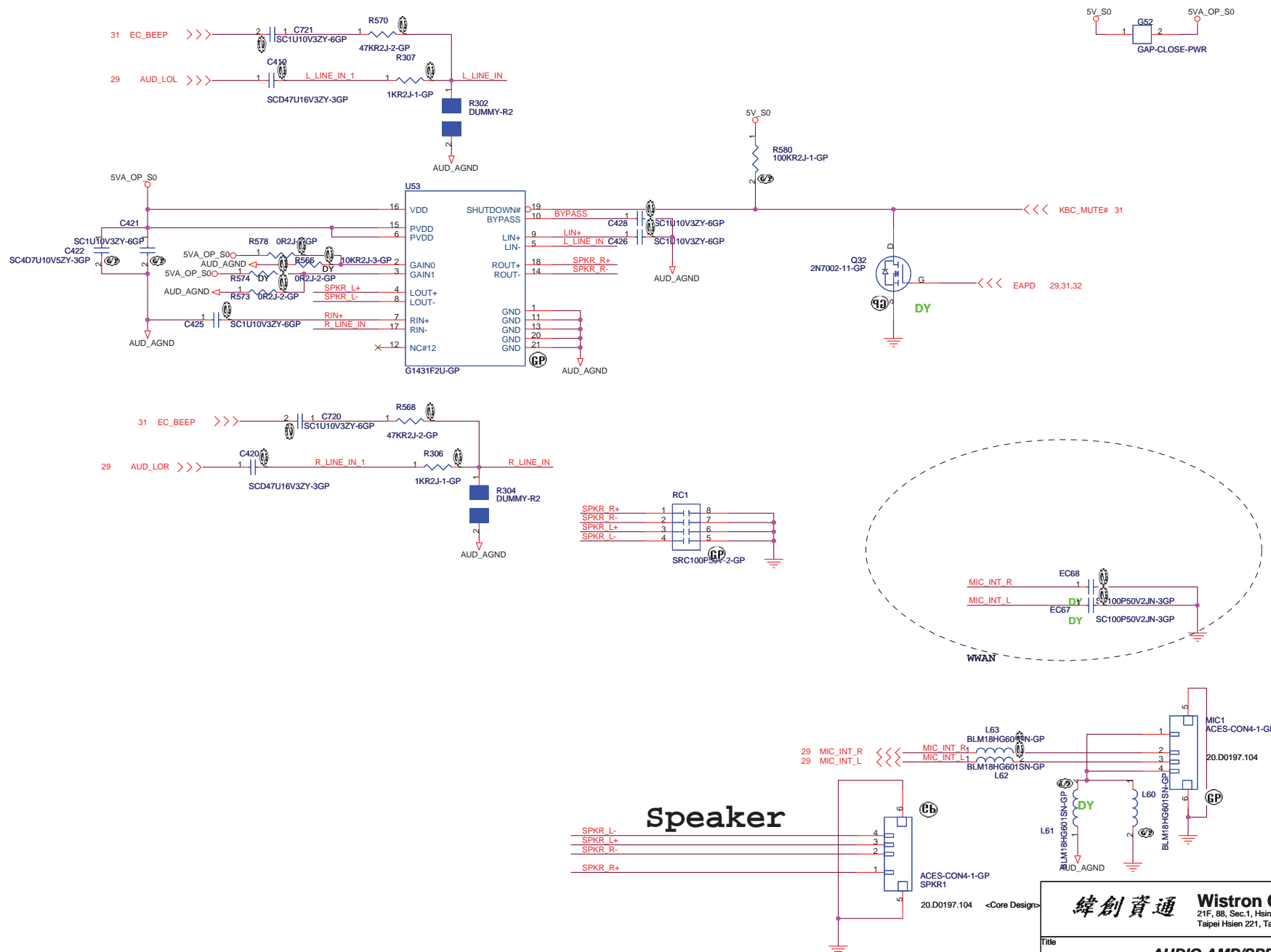


For Newcard socket



Title		LAN connector/NEW CARD/SIM	
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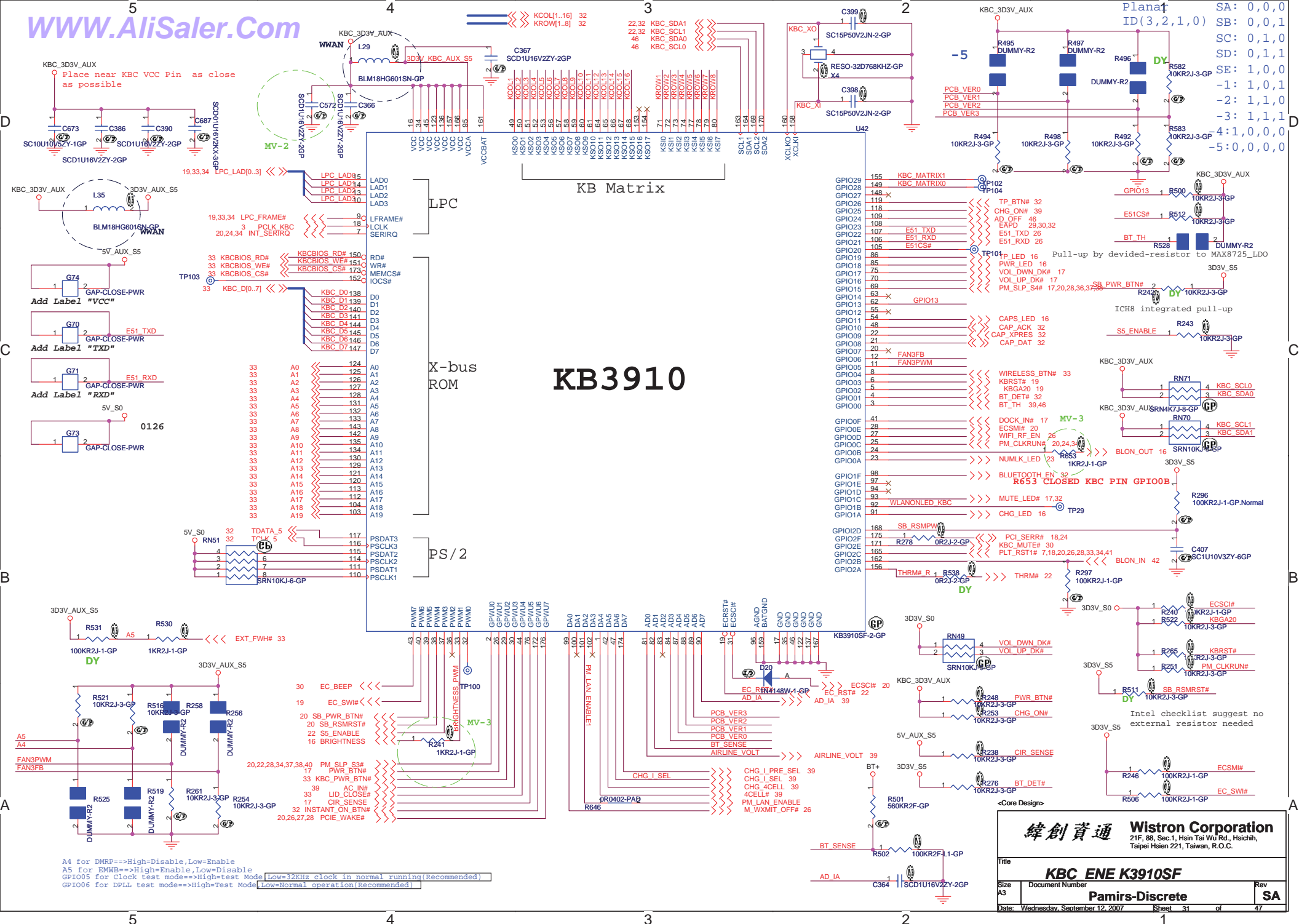




Speaker

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Title		AUDIO AMP/SPEAKER	
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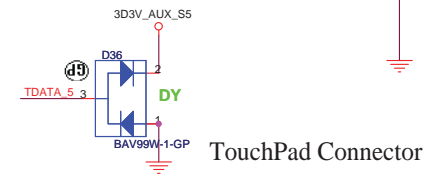


Internal Keyboard Connector

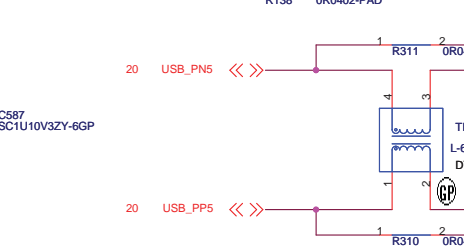
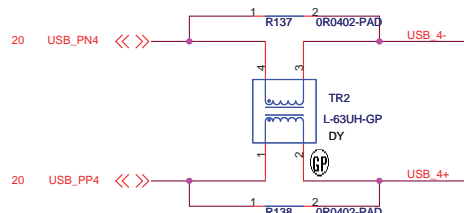
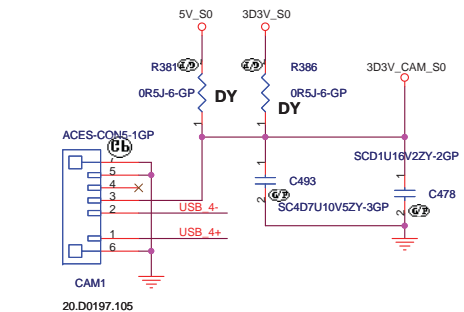
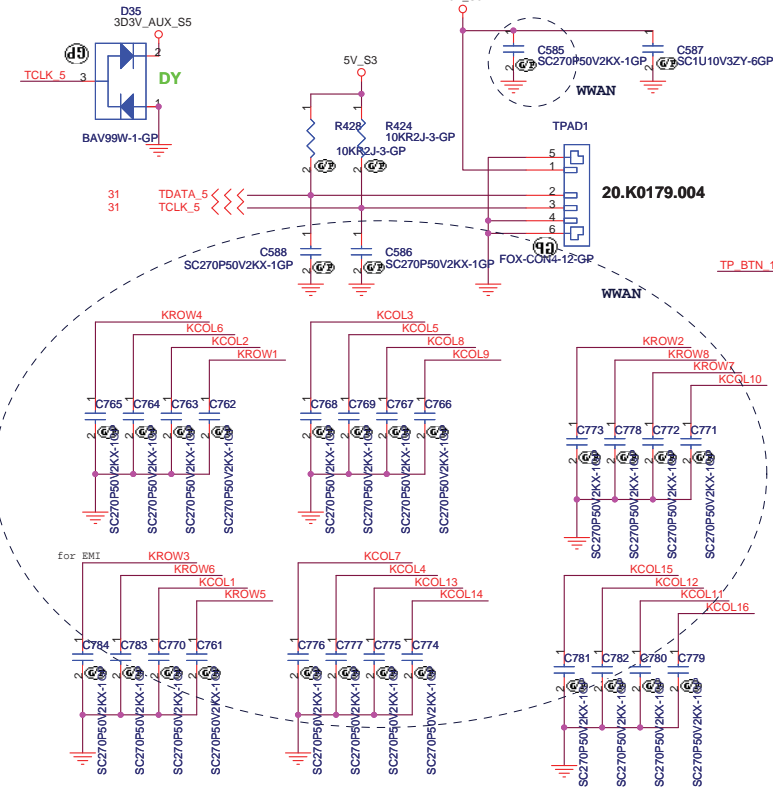
31 KROW1[1..8] <<< <<< <<<  
31 KCOL1[1..16] <<< <<< <<<

Keyboard matrix ( from vendor )

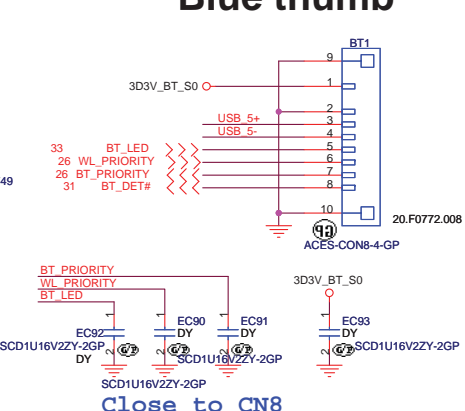
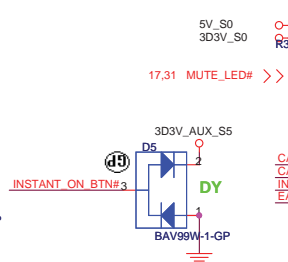
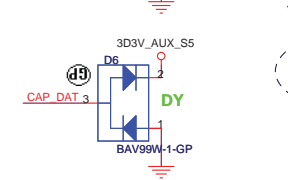
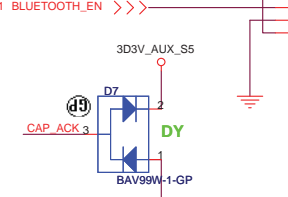
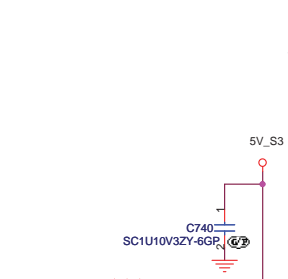
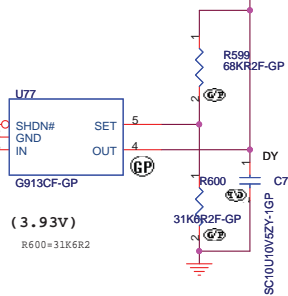
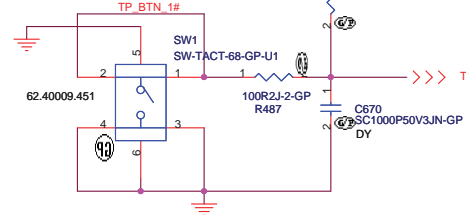
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



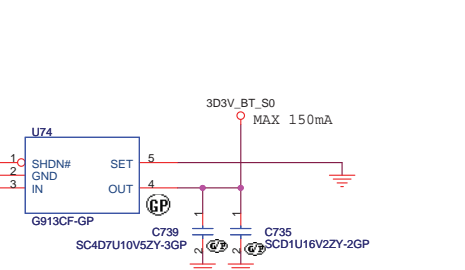
TouchPad Connector



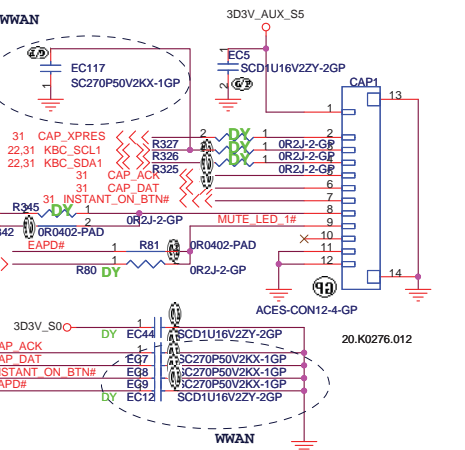
TOUCH-PAD SWITCH



Close to CN8



CAPACITY BUTTON

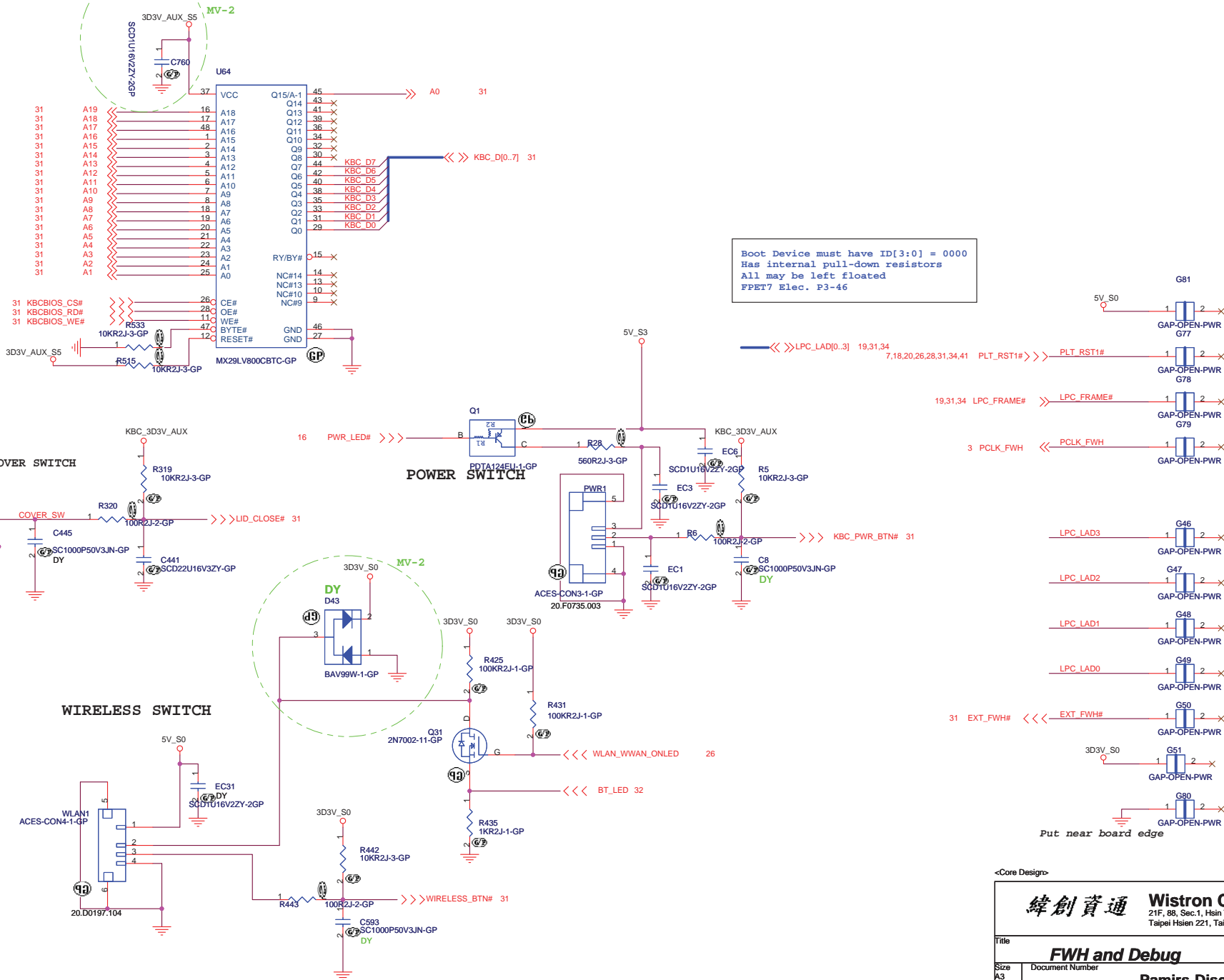


<Core Design>

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KeyBoard-CONN			
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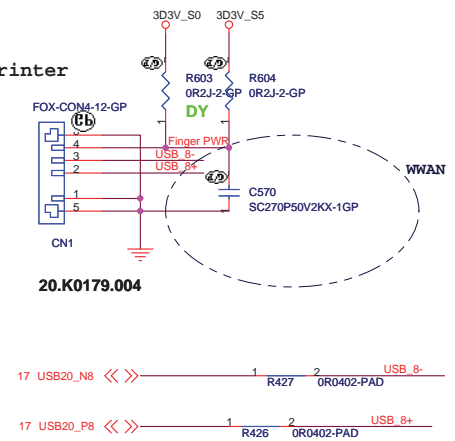
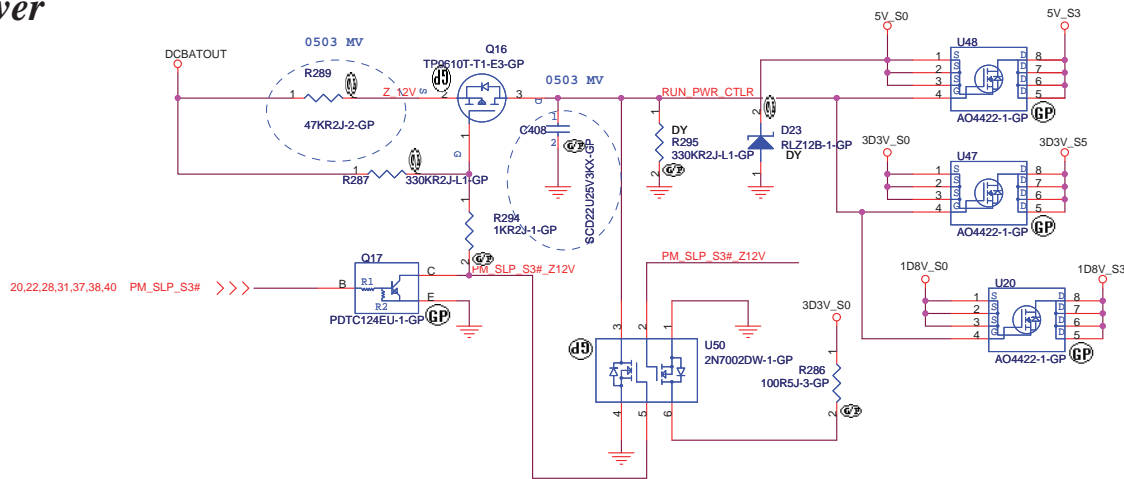
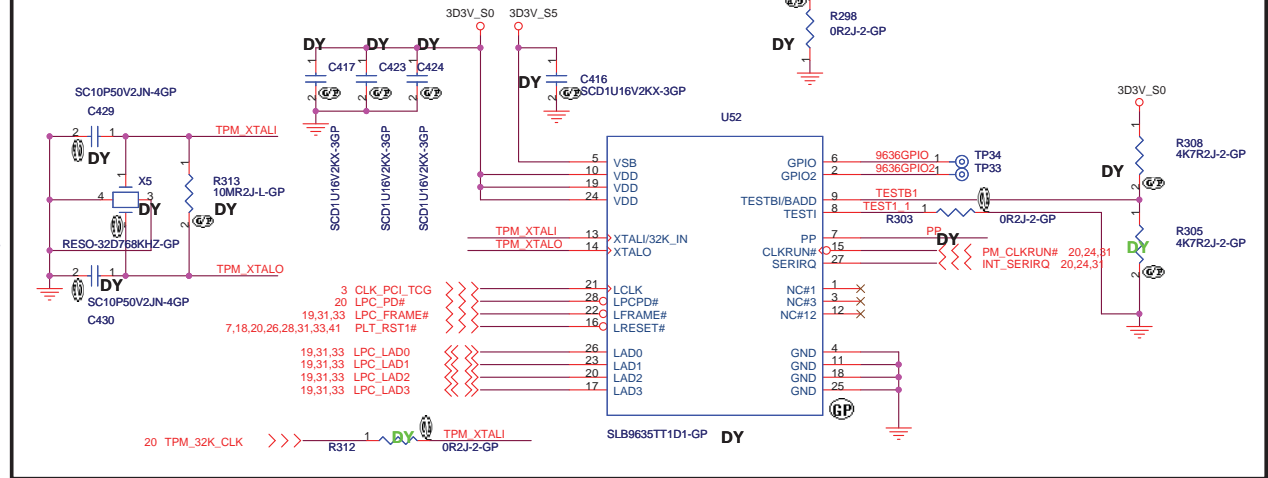
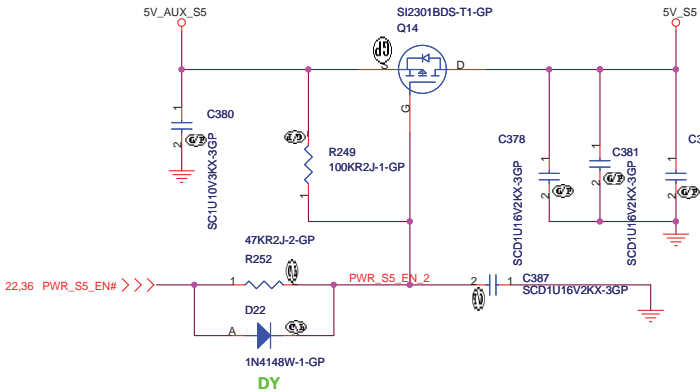
<Core Design>

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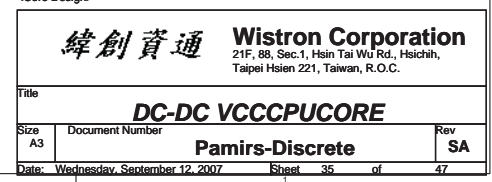
Title: **FWH and Debug**

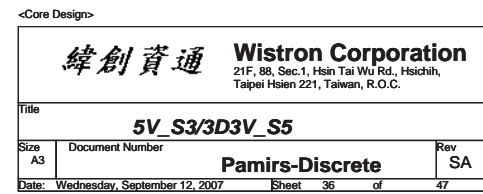
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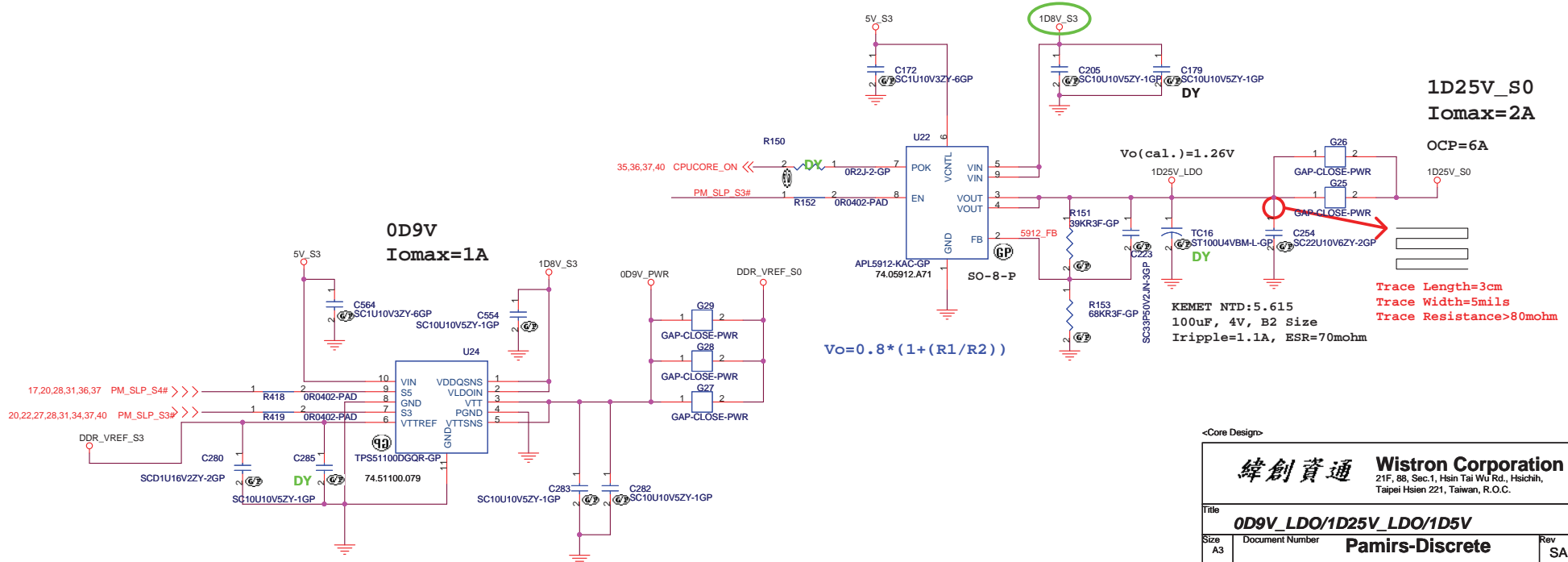
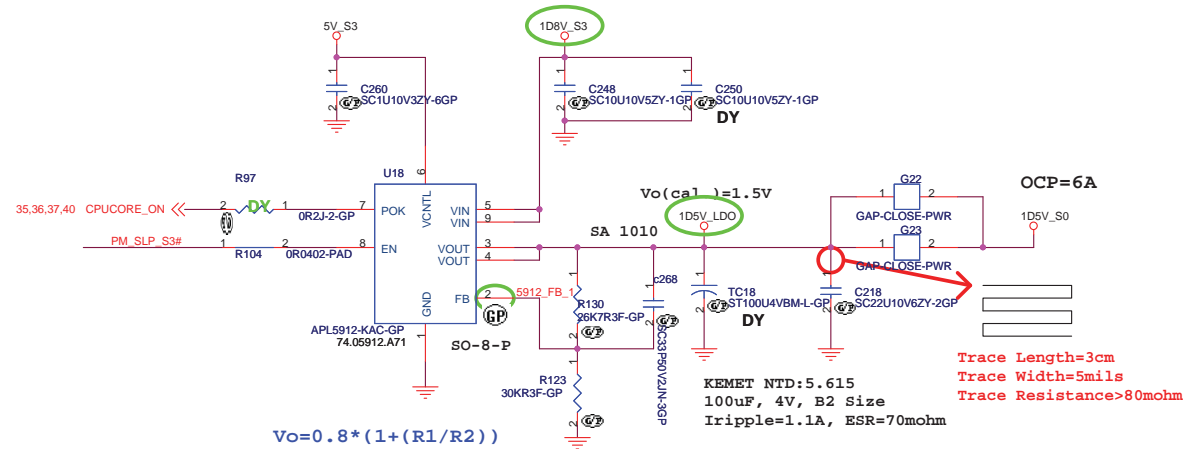


Title			
<b>PWRPLANE&amp;RESETLOGIC</b>			
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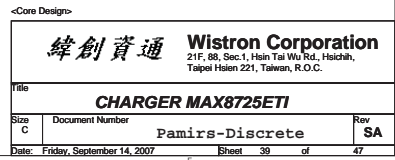


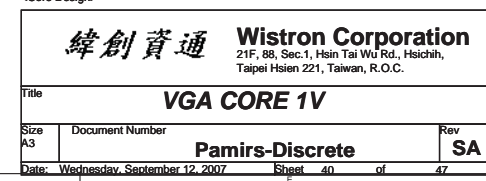


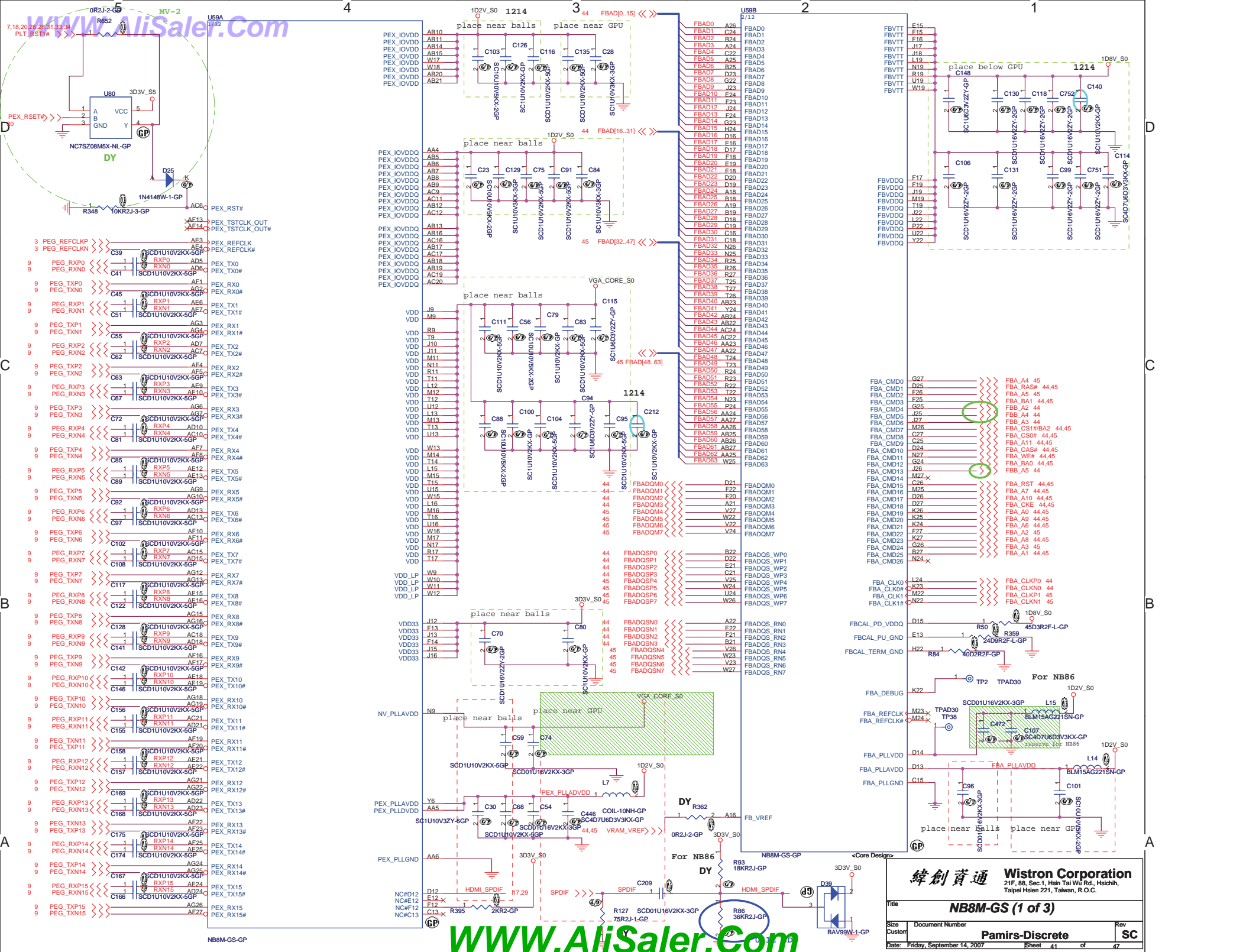


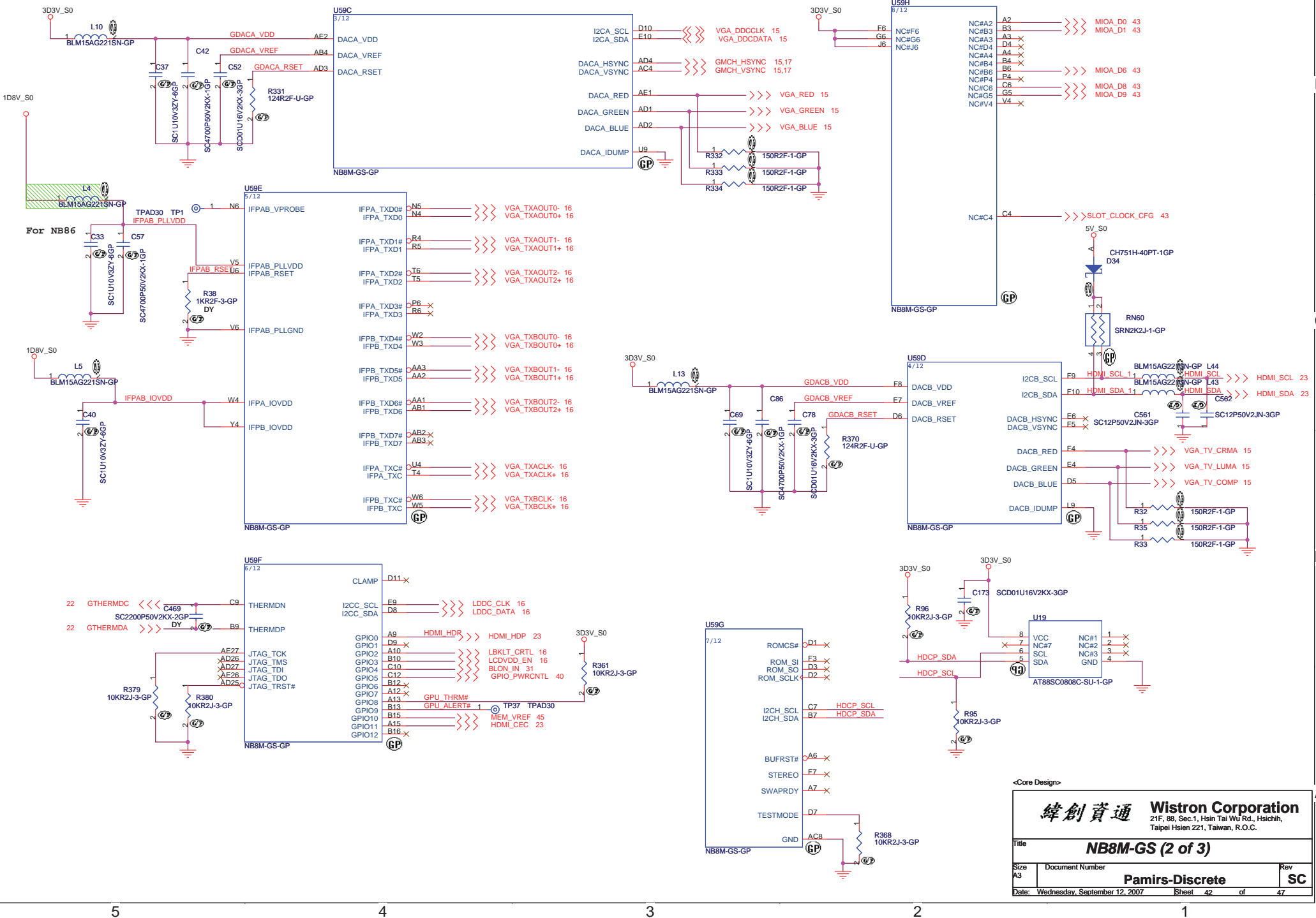
<Core Design>			
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Title			
0D9V_LDO/1D25V_LDO/1D5V			
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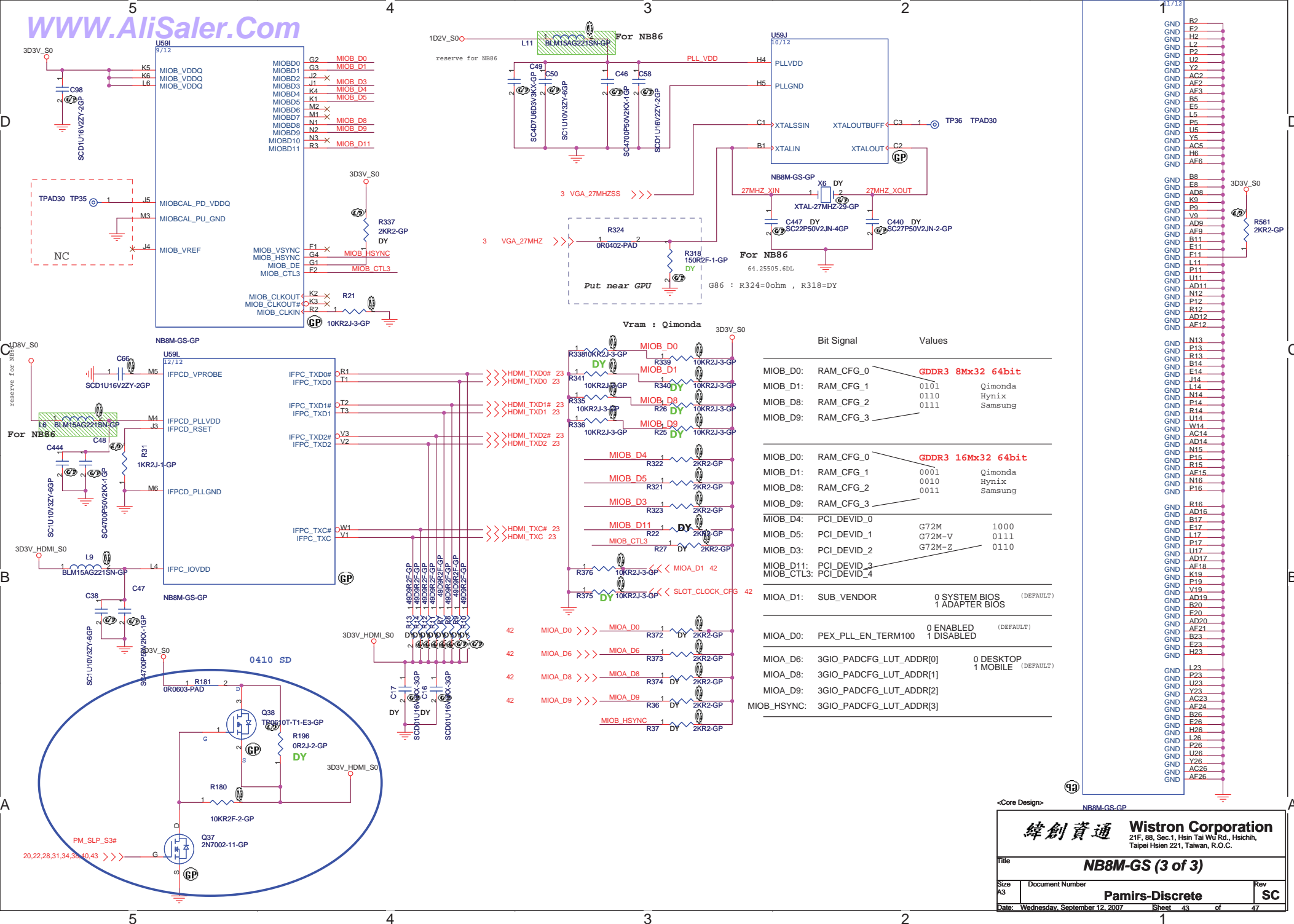




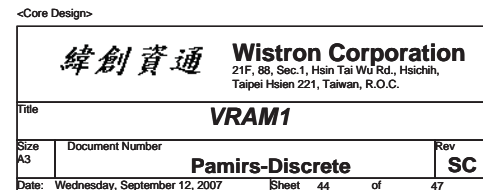


















Title			
<b>AD/BATT CONN</b>			
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